

PWA : Y507R
PWB : Y509R
SCH : Y510R

Calpella Intel Discrete Block Diagram

VER : E3B

POWER

AC/BATT CONNECTOR	PG 55
BATT CHARGER	PG 45

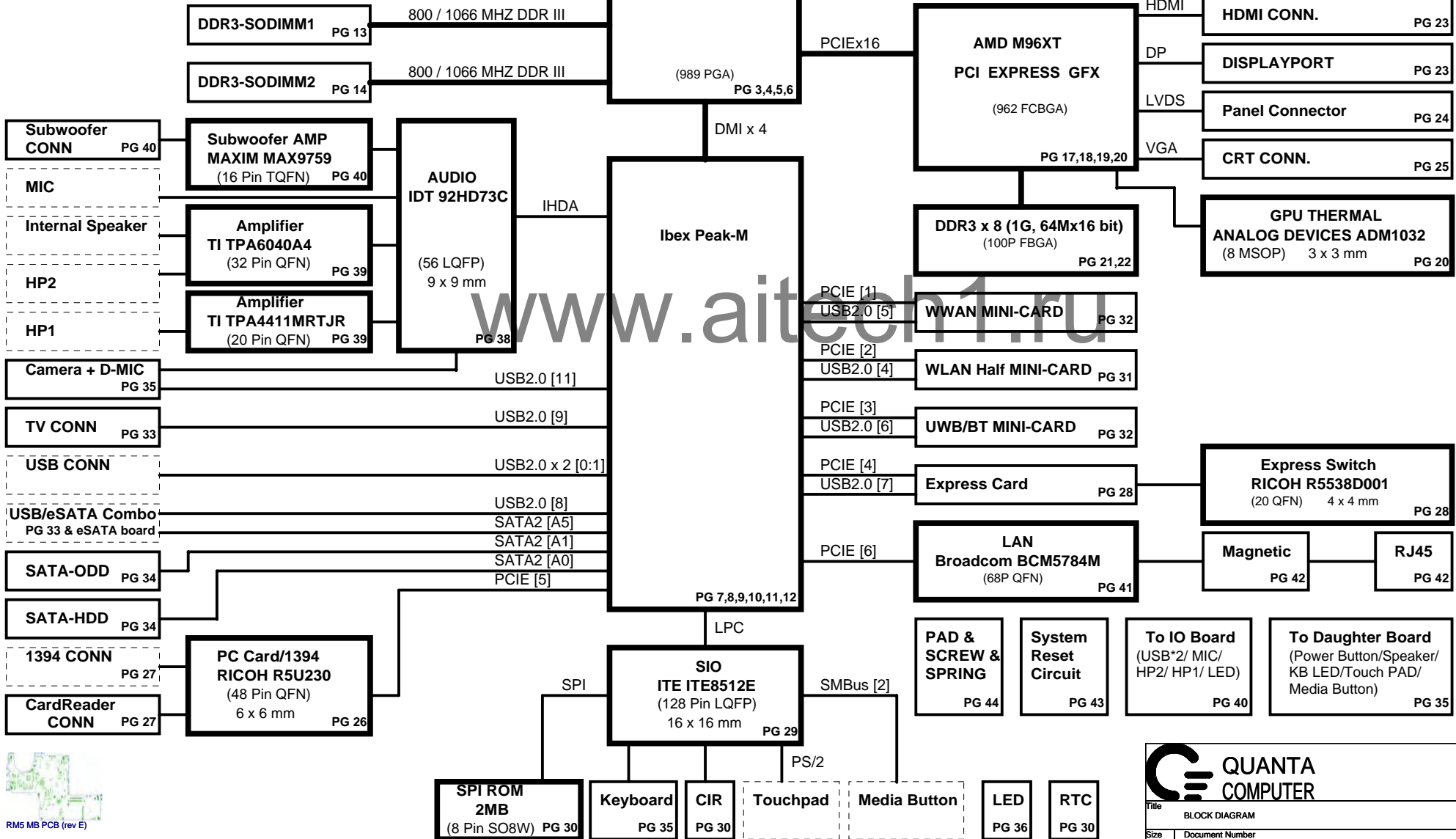
CLOCK SLG8SP585V (QFN-64)	PG 15
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FAN & THERMAL EMC1422 (8P TSSOP)	PG 37
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Clarksfield (Qual Core)

SYSTEM POWER

PCH REGULATOR +1.05V_PCH PG 49	SYS VR +5V_ALW2/+3.3V_ALW +5V_ALW/+15V_ALW PG 51	VGA Core +VCC_GFX_CORE +1.1V_GFX_PCIE PG 52
DDR3 VR +1.5V_SUS/+0.75V_DDR_VTT PG 47	CPU VR +1.1V_VTT PG 48	REGULATOR +1.8V_RUN PG 46
Load Switch +5V_SUS/+3.3V_SUS/+5V_RUN/ +3.3V_RUN/+1.5V_RUN/ +1.5V_GDDR PG 54	VCC Core +VCC_CORE PG 50	VGA VDDCI +VDDCI PG 53







Title	BLOCK DIAGRAM
Size	Document Number Calpella
Date	Thursday, October 01, 2009
Sheet	1 of 61
Rev	3B

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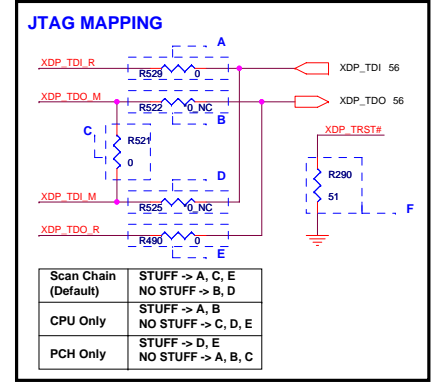
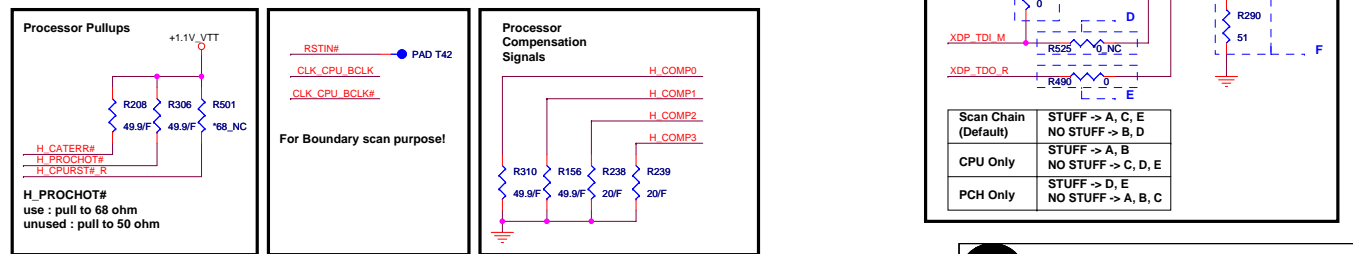
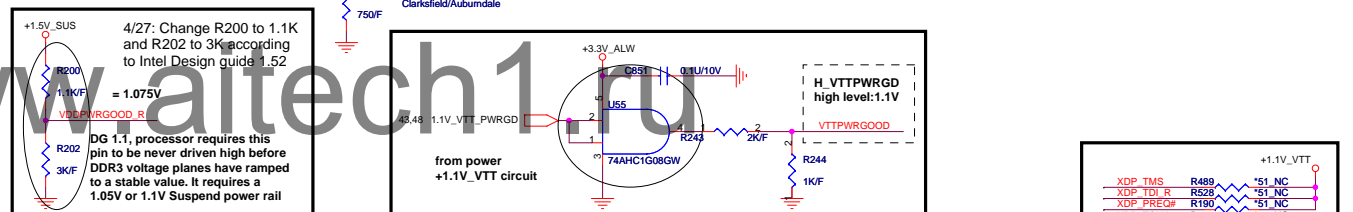
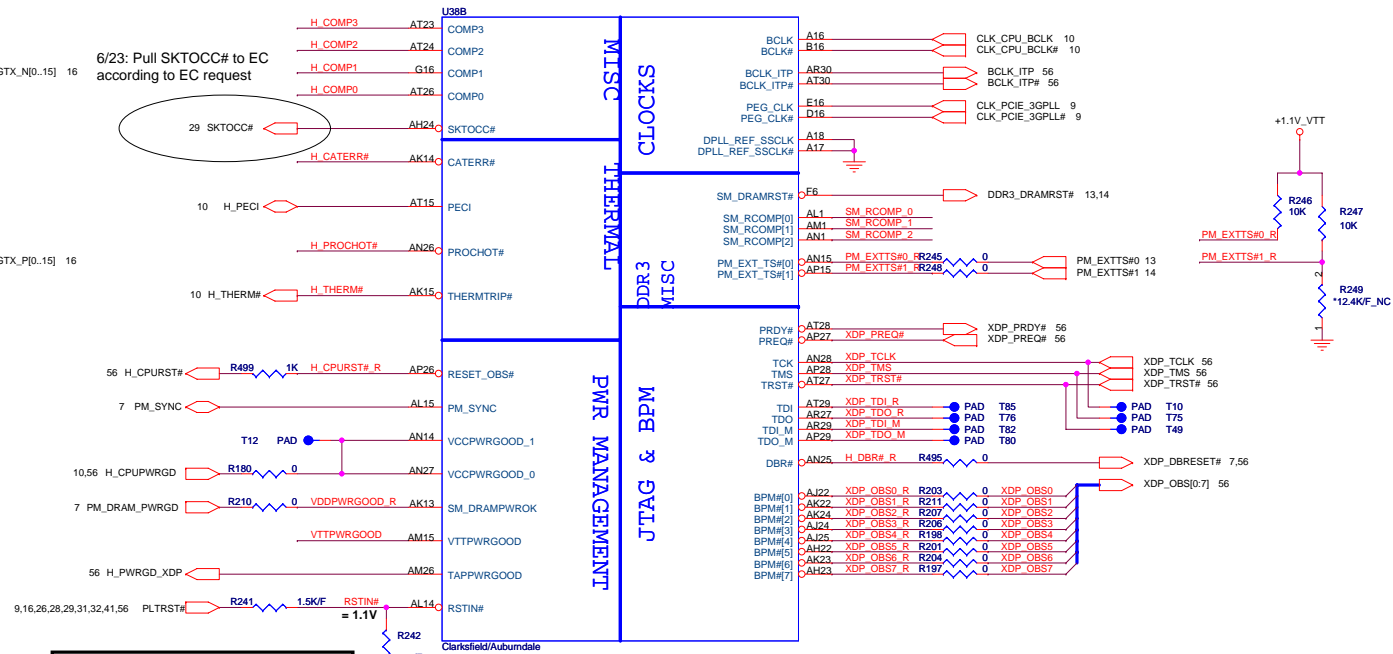
PAGE	DESCRIPTION
1	Block Diagram
2	Front Page
3-6	CPU (Clarksfield)
7-12	PCH (IBex Peak-M)
13-14	DDR3 SO-DIMM(204P)
15	Clock Generator
16-22	GPU (M96XT)
23	HDMI & DP
24	LCD connector
25	CRT
26	Card reader PCIe interface
27	Card reader & 1394 CONN
28	Express card
29	SIO (IT8512)
30	Flash/RTC/CIR
31	WLAN
32	WWAN/WPAN
33	USB & eSATA & TV
34	SATA HDD & ODD
35	KB/CCD/UI
36	LED
37	FAN/Thermal
38-40	Audio/CONN/Subwoofer (92HD73C).
41-42	LAN/RJ45 (BCM5784M)
43	System Reset Circuit
44	PAD & SCREW & SPRING
45	CHARGER (MAX8731A)
46	1.8V_RUN (TPS51218)
47	1.5_SUS/0.75(TPS51116)
48	1.1V_VTT(TPS51218)
49	1.05V_PCH (TPS51218)
50	VCC_CORE(MAX17036GTL+)
51	3.3V/5V/15V (MAX17020)
52	VGA_M97(MAX8792)
53	VDDCI_M97(TPS51218)
54	Run Power Switch
55	DCIN & Batt
56	XDP Connector
57	Power Block Diagram
58	SMBUS BLOCK
59	Power status

Power States

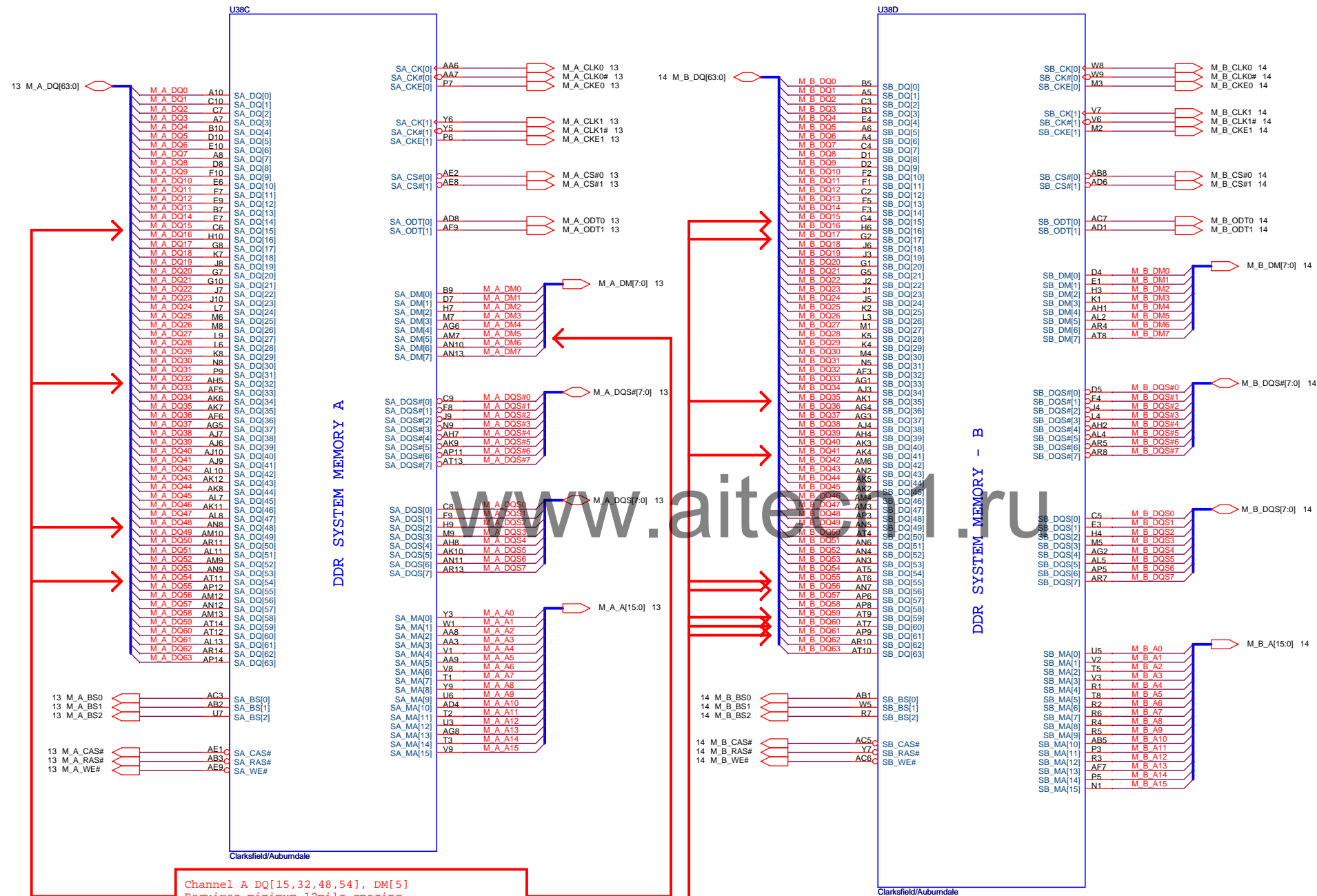
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51,52,53	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	8,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,29,30,34,35,36,43,45,51,54,55	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	24,33,34,35,47,51,52,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	24,34,51,54	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	41,42	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,46,48,49,52,53,54	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,8,9,10,11,20,24,28,29,42,43,46,47,48,49,52,53,54	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.5V_SUS	+1.5V	3,5,13,14,47,52,54	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,54	SODIMM POWER	SUS_ON	
+5V_RUN	+5V	11,18,23,25,33,35,36,37,38,50,54	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	7,8,9,10,11,13,14,15,18,23,24,26,28,29,30,31,32,33,34,35,36,37,38,39,40,41,50,52,54,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	5,11,17,18,19,46,54	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	28,31,32,54	PCH POWER	1.5V_RUN_ON	
+1.1V_VTT	+1.1V	3,5,10,11,48,50,56	CPU POWER	RUN_ON	
+1.05V_PCH	+1.05V	8,9,11,15,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.5V	5,50	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	34	Module Power	MODC_EN#	
+5V_HDD	+5V	34	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	35,36,51,54,55	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
 AGND	38,39,40	
 AGND_DC/DC	51	
 AGND_VCORE	50	
 GND	ALL	

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

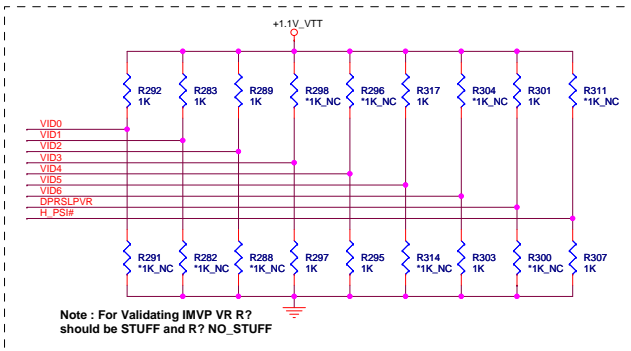
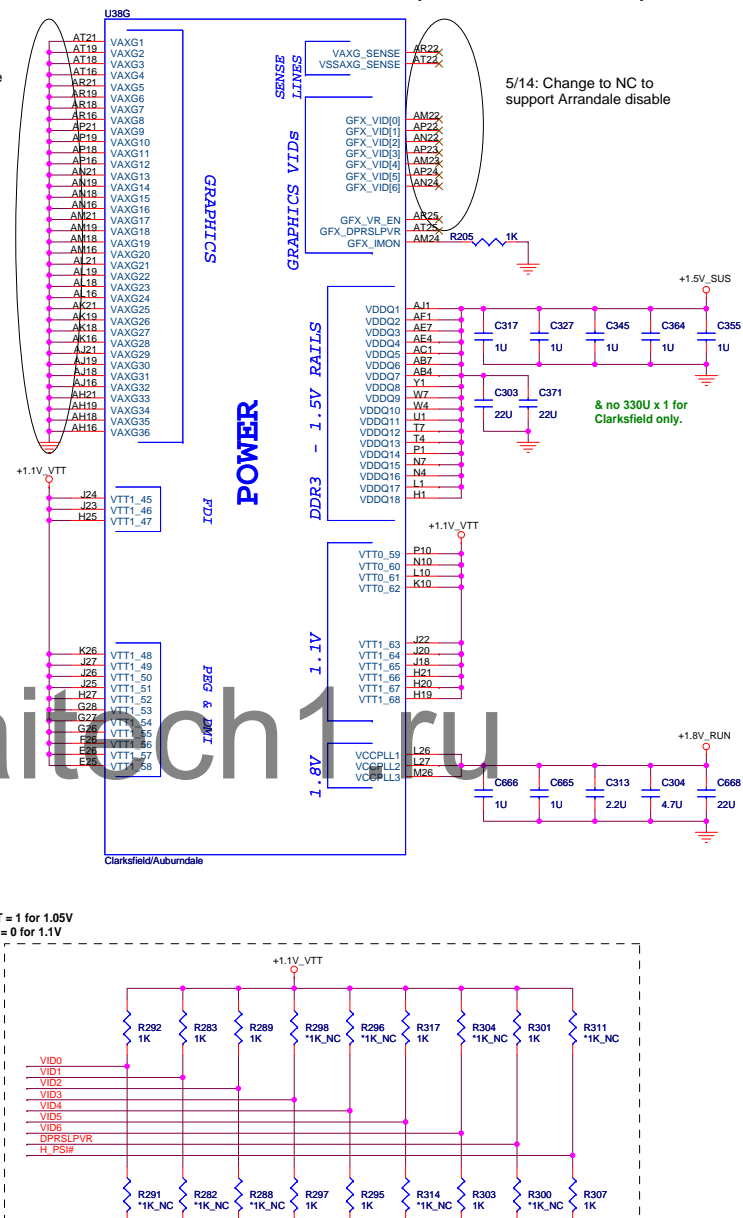


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



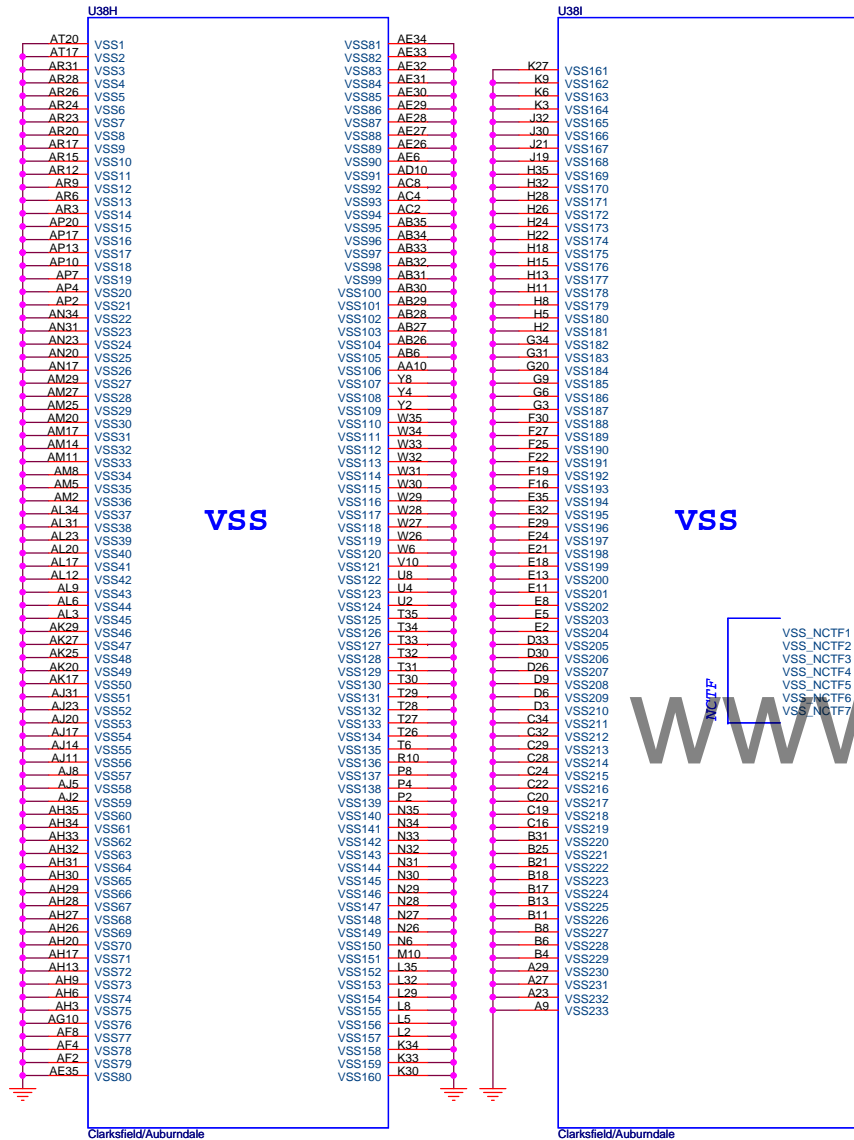
Title			CPU 2/4(DDR)
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AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

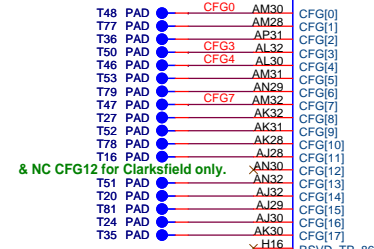
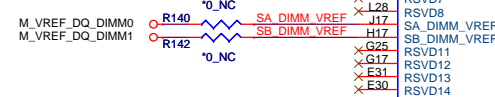


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

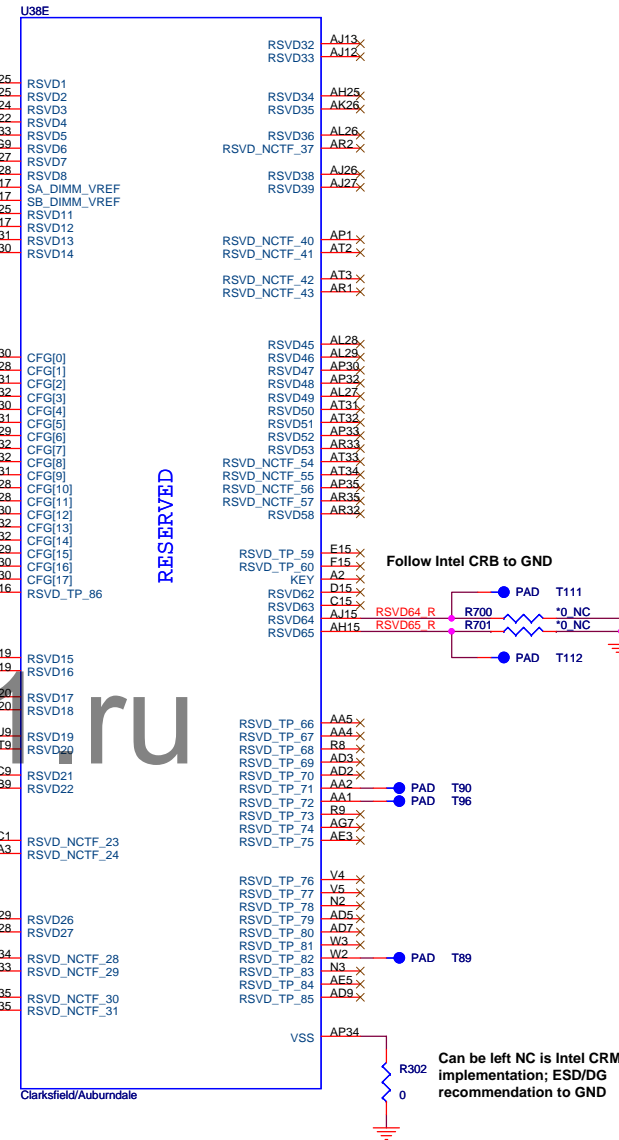
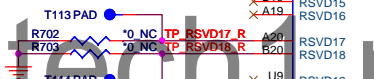


Processor Generated
SO-DIMM VREF_DQ (M3)
Connect to page 13, 14



& NC CFG12 for Clarkfield only.

Follow Intel CRB to GND

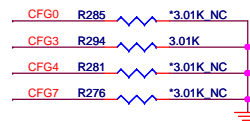


Follow Intel CRB to GND



Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

Scott_0630:Change R294 footprint from RC0402-C to RC0402



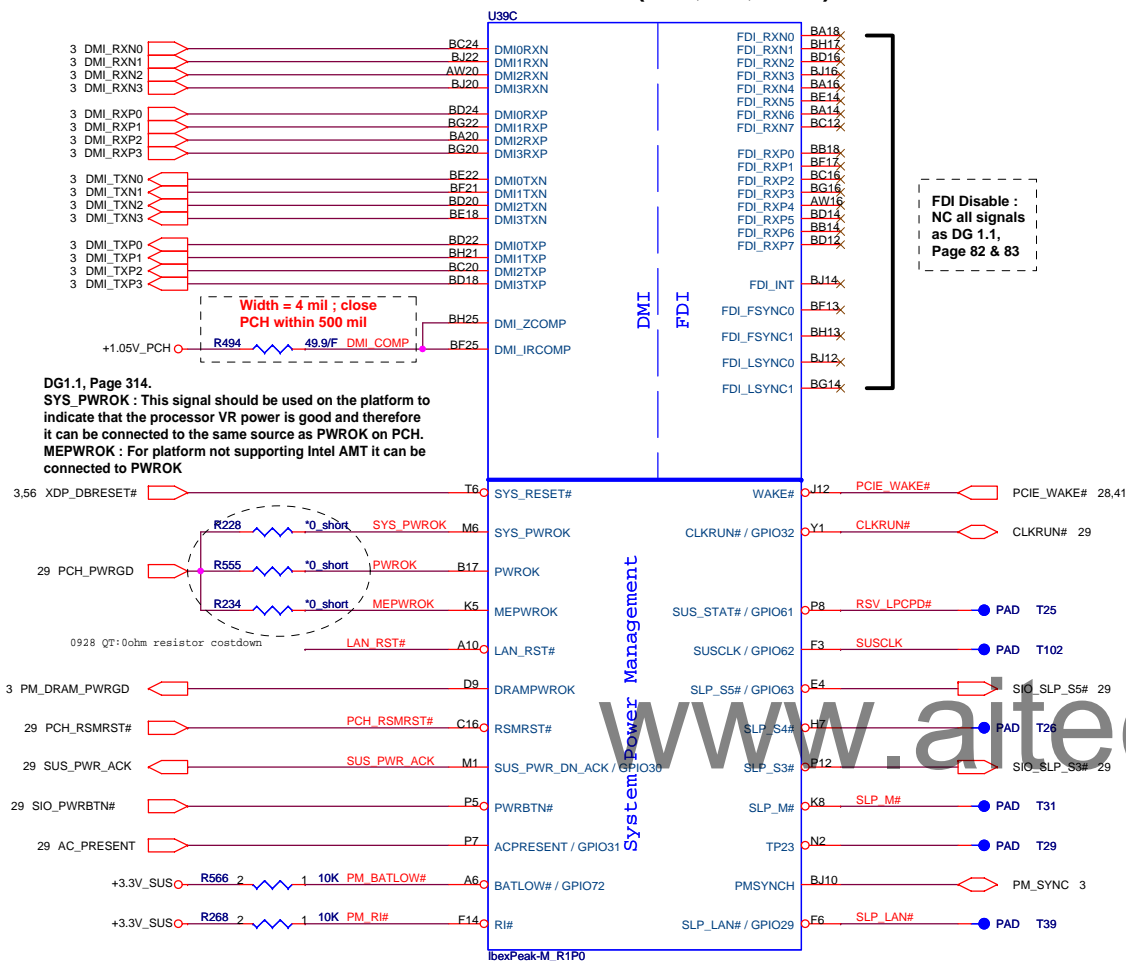
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG0 (PCI-Epress Configuration Select)	Single PEG (Default)	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation (Default)	Lane Numbers Reversed
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port (Default)	Enabled; An external Display port device is connected to the Embedded Display port
CFG7 Clarkfield (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD (Default)



Title CPU 4/4(GND_RESV)		
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IBEX PEAK-M (DMI,FDI,GPIO)

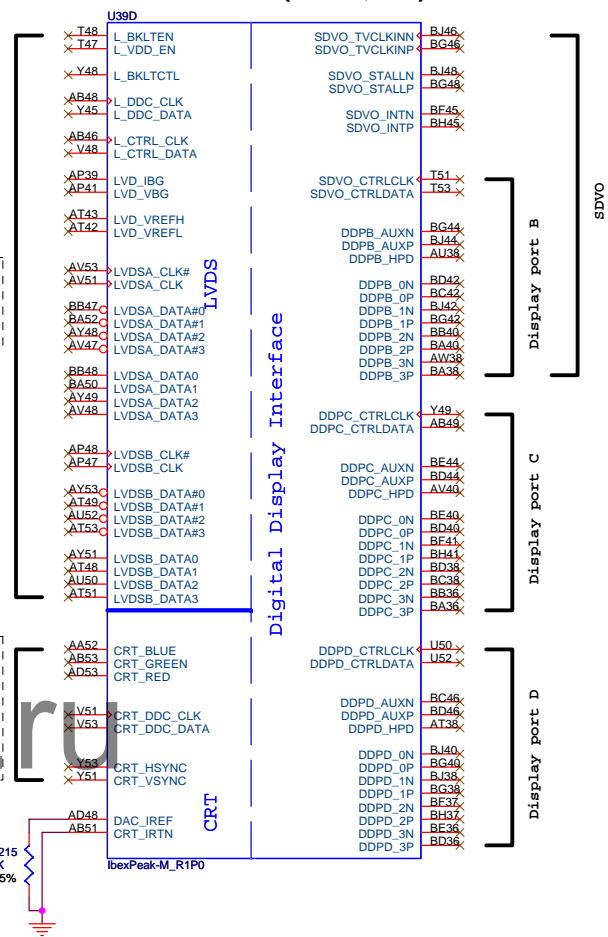


FDI Disable :
NC all signals
as DG 1.1,
Page 82 & 83

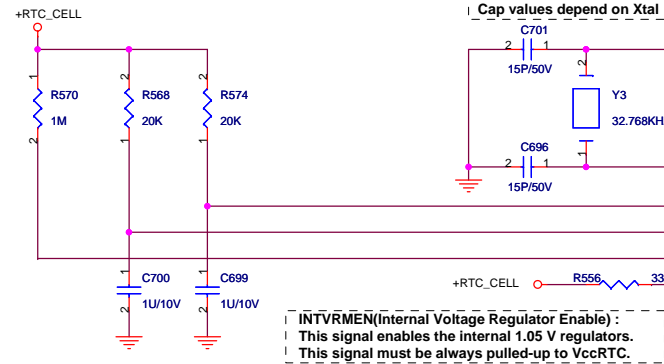
LVDS Disable :
All signals associated
with the interface can
be left as No connects.

CRT Disable :
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_HSYCN
CRT_VSYN
Leave as NC (floating).

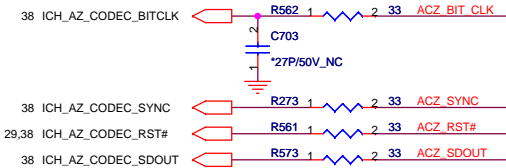
IBEX PEAK-M (LVDS,DDI)



IBEX PEAK-M (HDA,JTAG,SATA)



INTVRMEN(Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

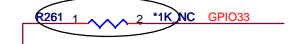
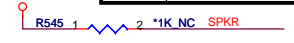


Place all series terms close to PCH (within 500 mil) except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot strap.

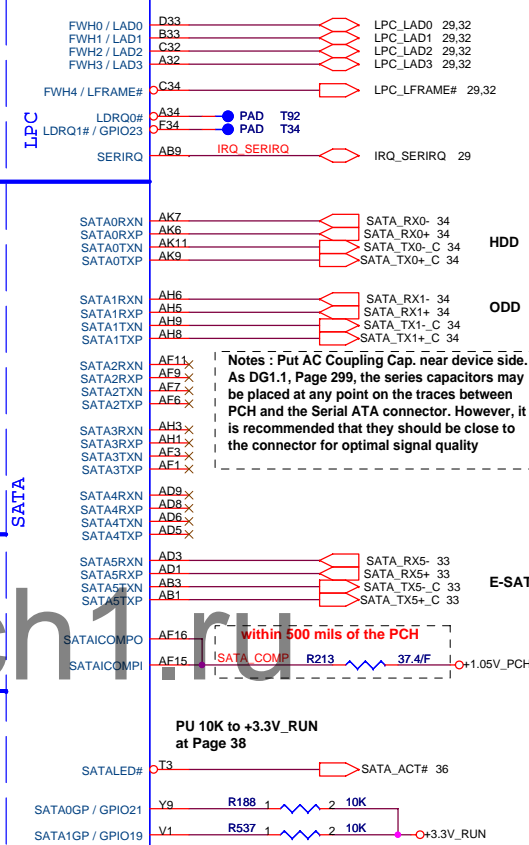
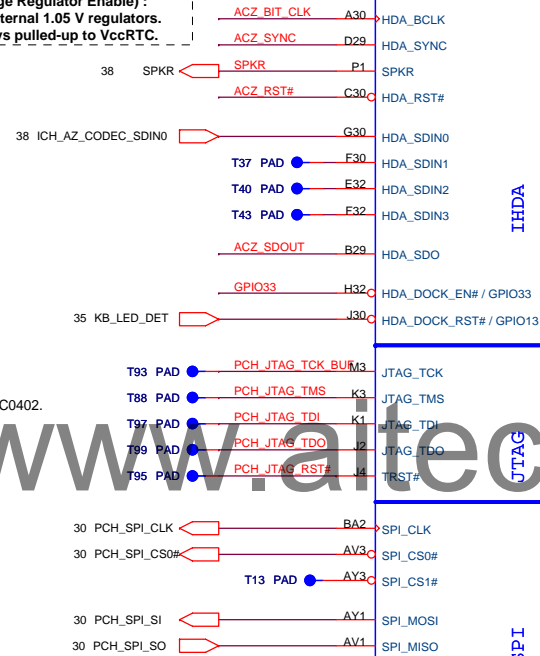
SPKR Low = Default.
High = No Reboot.

Scott_0630: Change R545 footprint from RC0402-C to RC0402.



Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

6/2: Change R261 from 10K_NC to 1K_NC according to Intel design guide 1.51



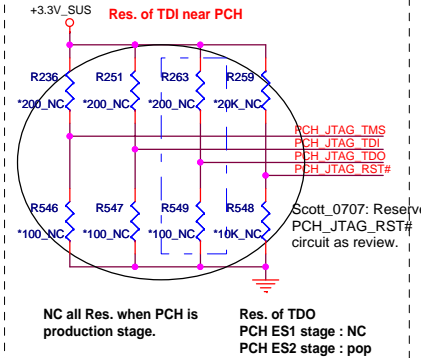
Notes : Put AC Coupling Cap. near device side.
As DG1.1, Page 299, the series capacitors may be placed at any point on the traces between PCH and the Serial ATA connector. However, it is recommended that they should be close to the connector for optimal signal quality

Notes : FIS-based Port Multiplier support on SATA Ports 4 and 5 in AHCI/RAID mode.

PU 10K to +3.3V_RUN at Page 38

within 500 mils of the PCH
SATA COMP R213 37.4/F +1.05V_PCH

6/2: NC JTAG resistors as PCH is in QT stage



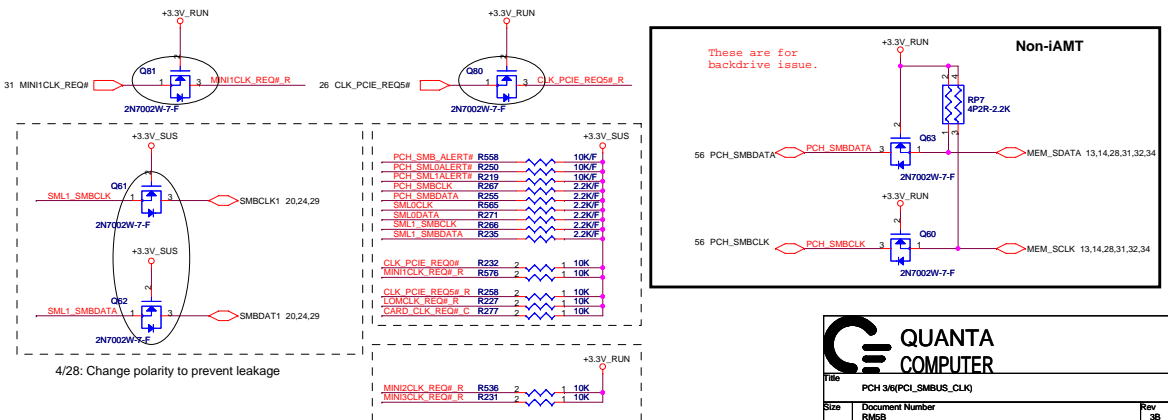
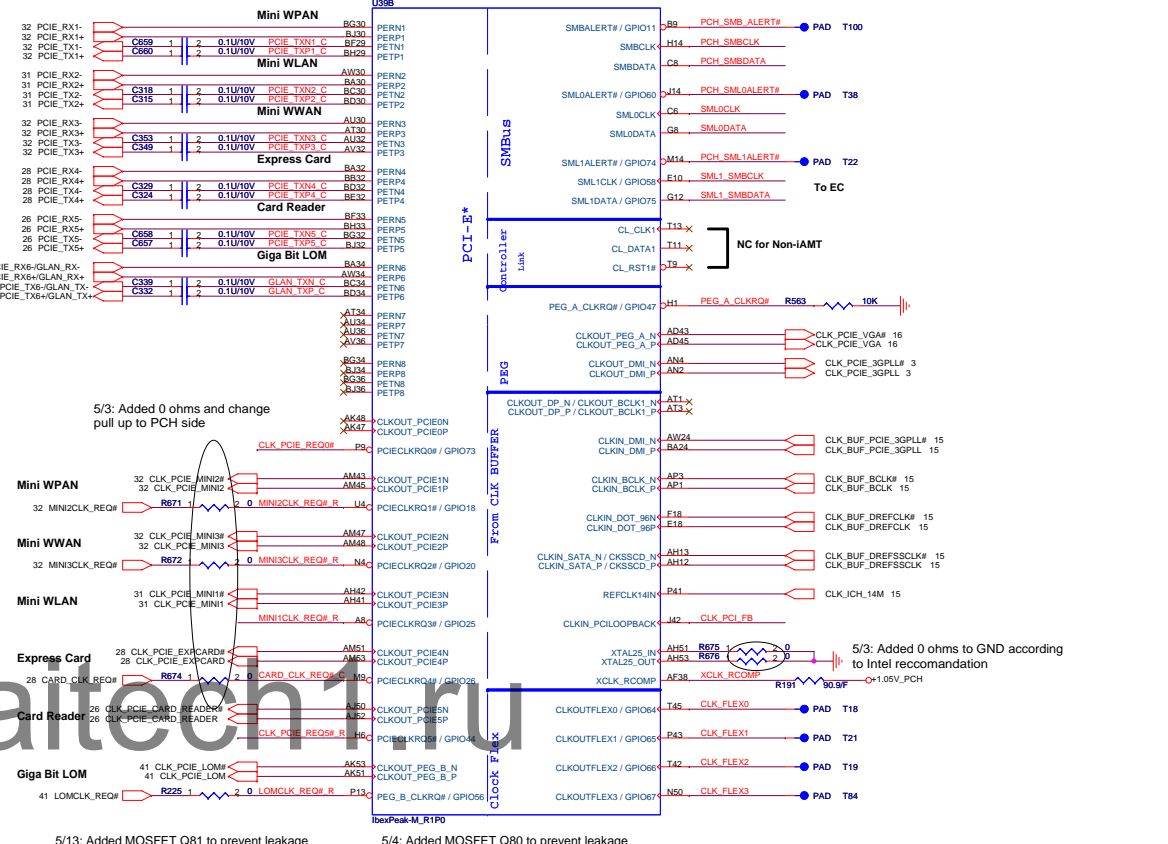
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Scott_0703 : Note : Delete pull up 1.05V according to Intel change notice! (Reserved for debug purpose)

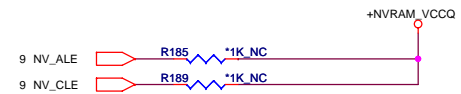
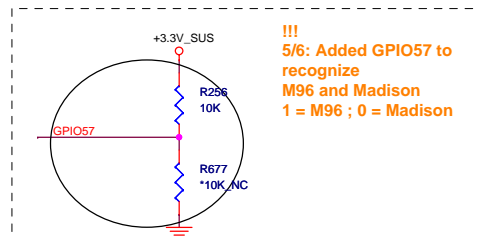
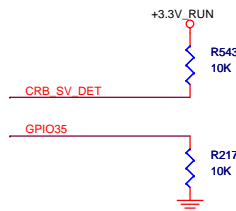
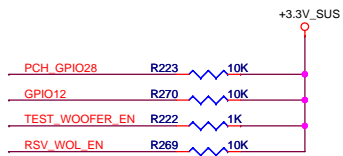
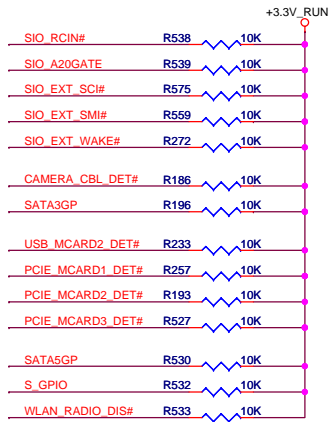
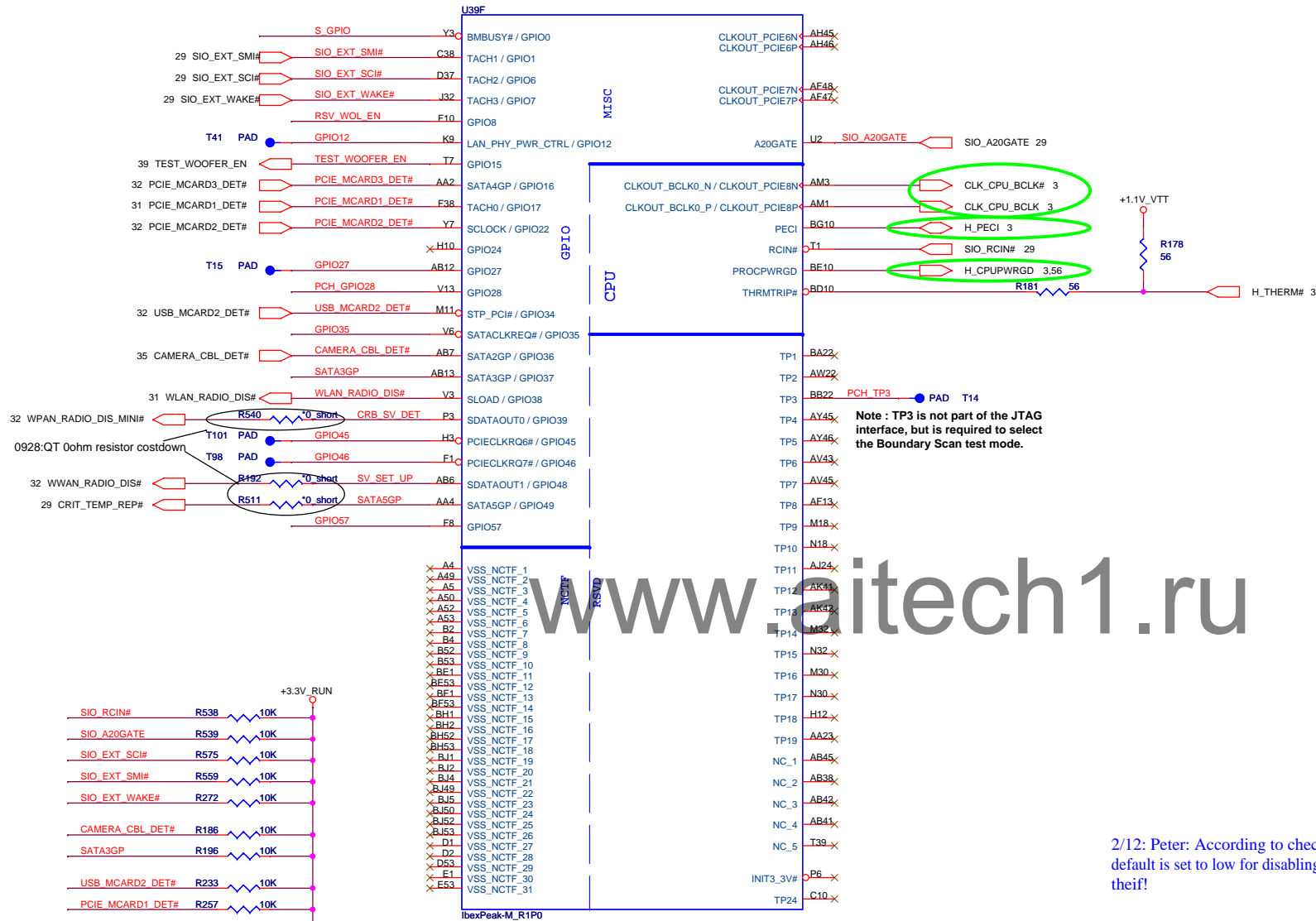


Title			PCH 2/6(SATA_SPI)
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IBEX PEAK-M (PCI-E,SMBUS,CLK)



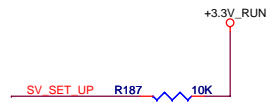
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

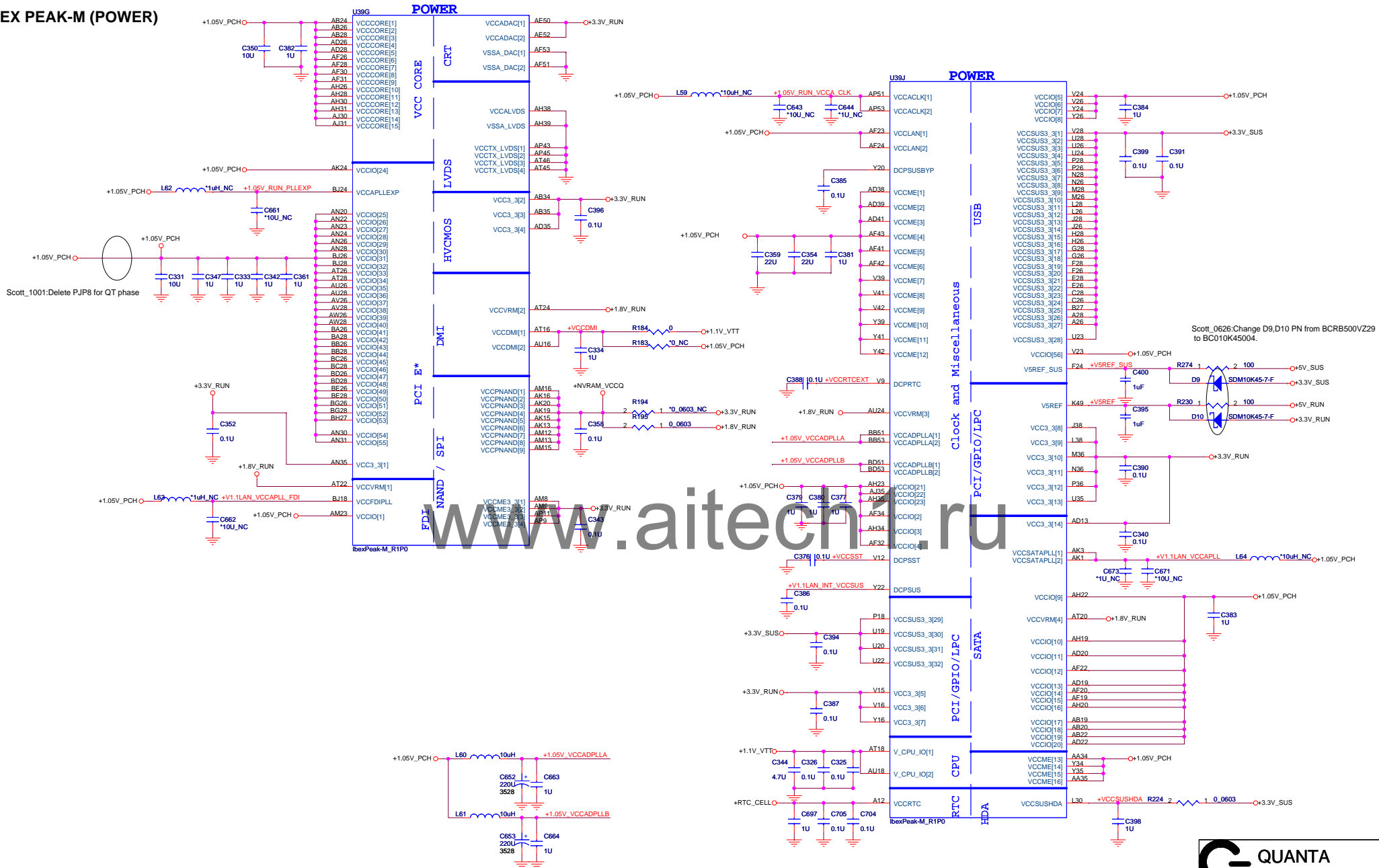
Anti-Theft Enabled	
NV_ALE	High = Enable (Default) Low = Disable

2/12: Peter: According to checklist, default is set to low for disabling anti-theif!



SV_SET_UP	1-X High = Strong (Default)
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IBEX PEAK-M (POWER)



Use External Graphics. Can connect power directly without Inductor & Cap ? As Ibex peak-M EDS 1.0, need +1.05V. Can use +1.1V_VTT as CPU ?



Title PCH 5/6(POWER)

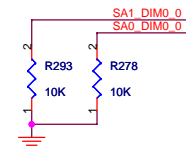
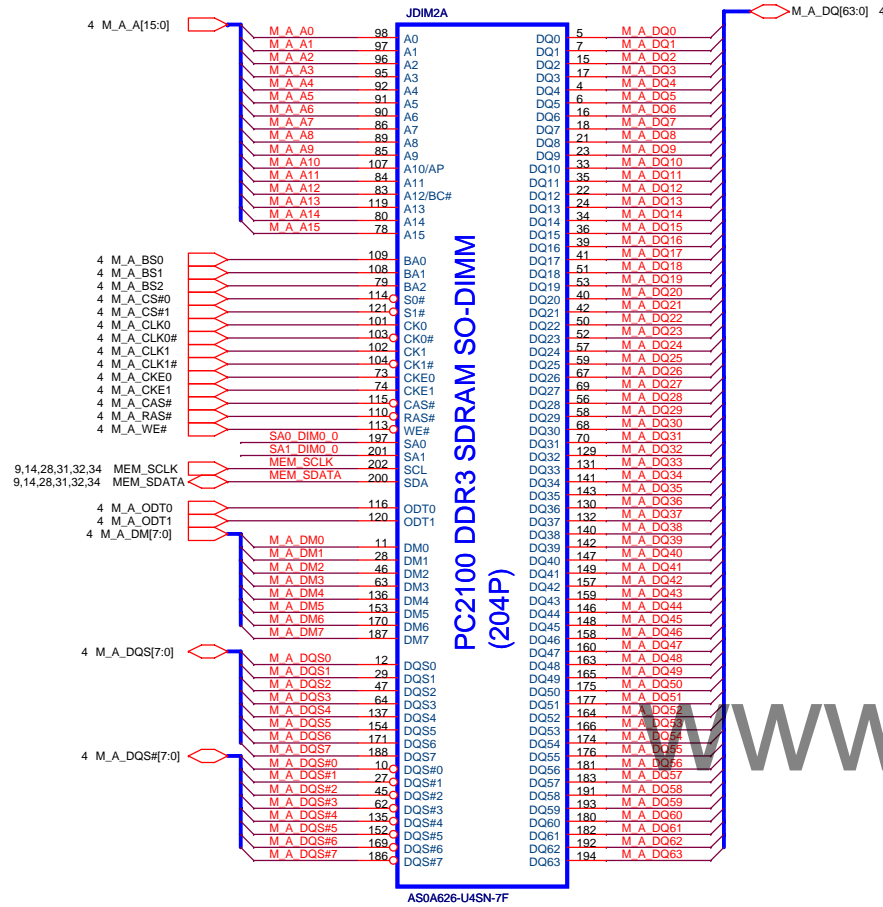
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IBEX PEAK-M (GND)



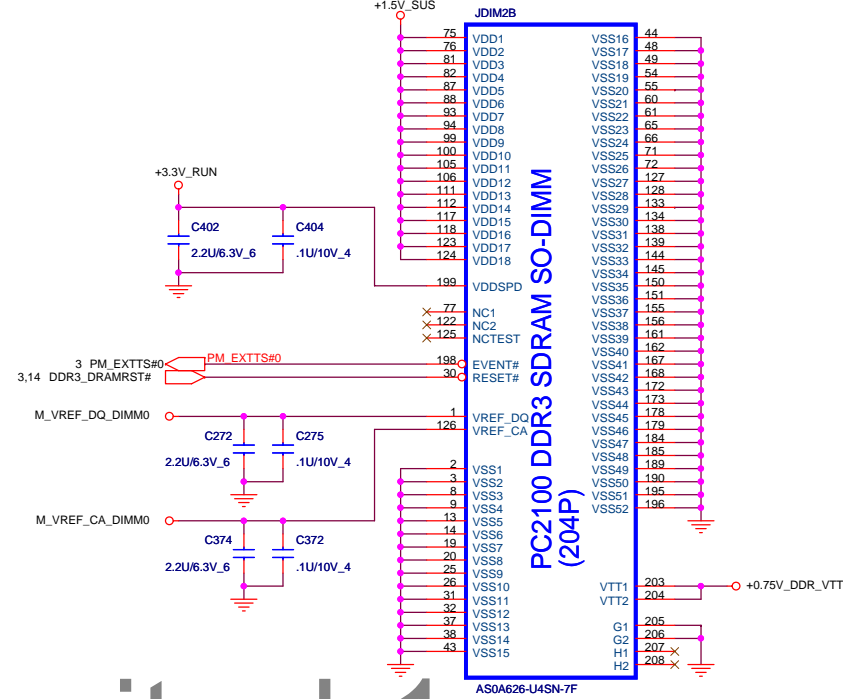
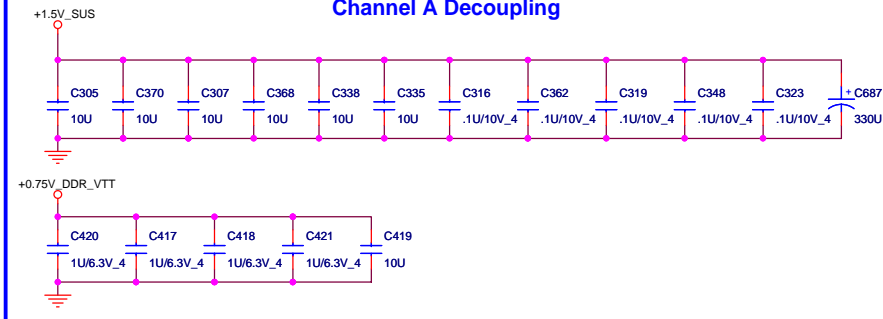
5/13: Change connector from Tyco to Foxconn to avoid shortage

Channel A



Note:
If SA1_DIM0 = 0, SA0_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA1_DIM0 = 0, SA0_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Channel A Decoupling



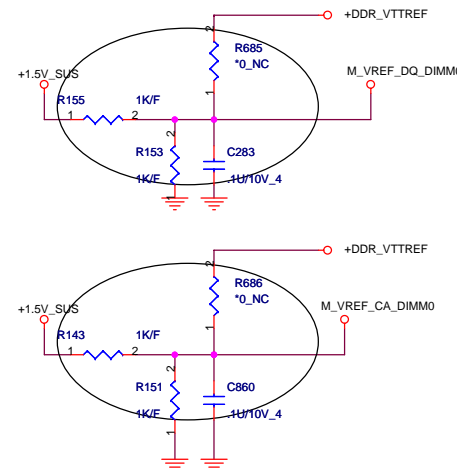
For CH A SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

5/18: Separate voltage divider for M_VREF_DQ_DIMM0 and M_VREF_CA_DIMM0 to follow Intel CRB design

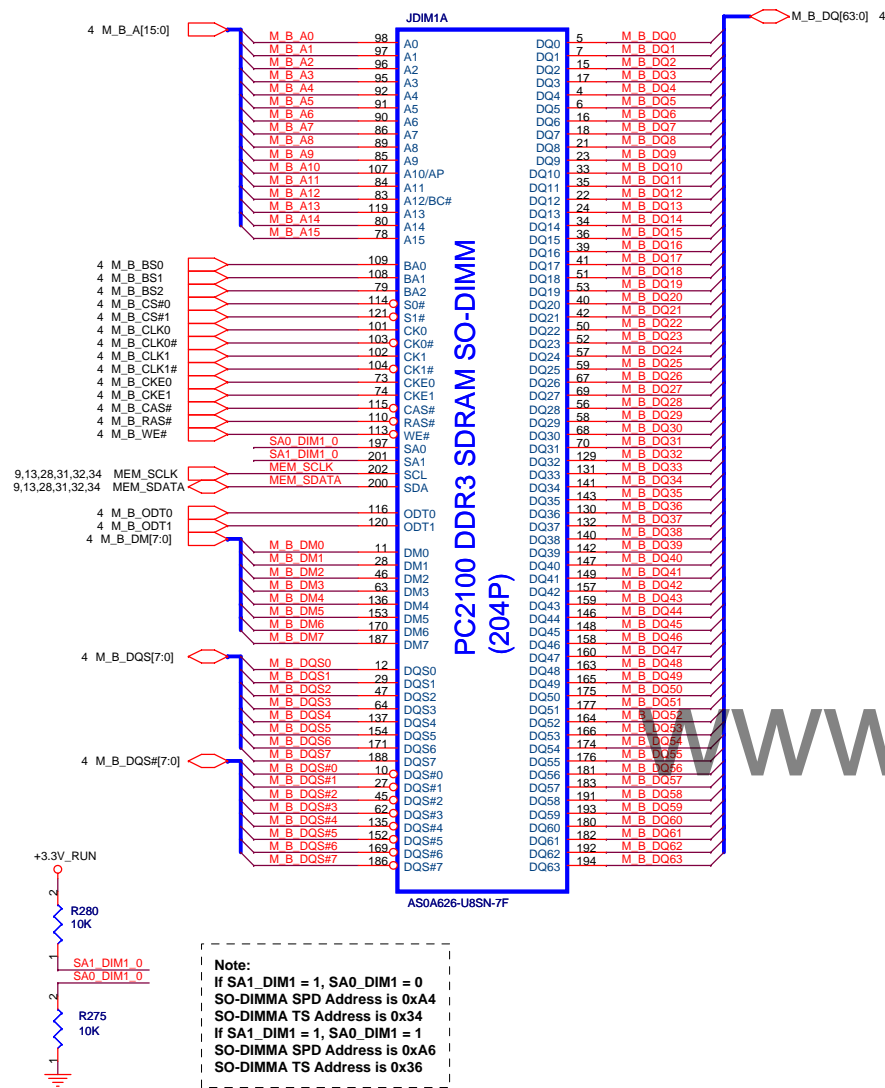
6/02: Change M1 from voltage regulator to voltage divider



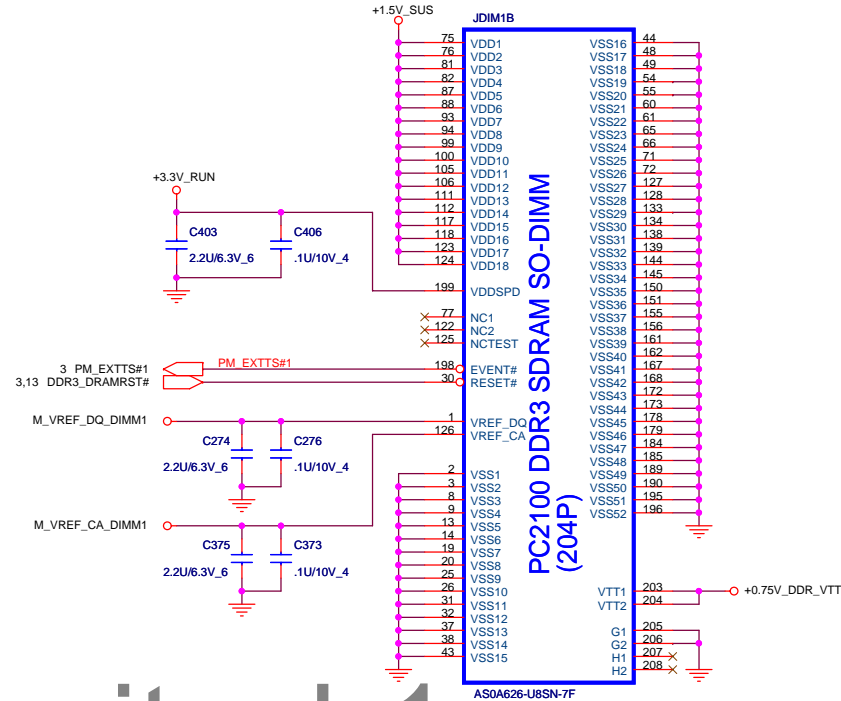
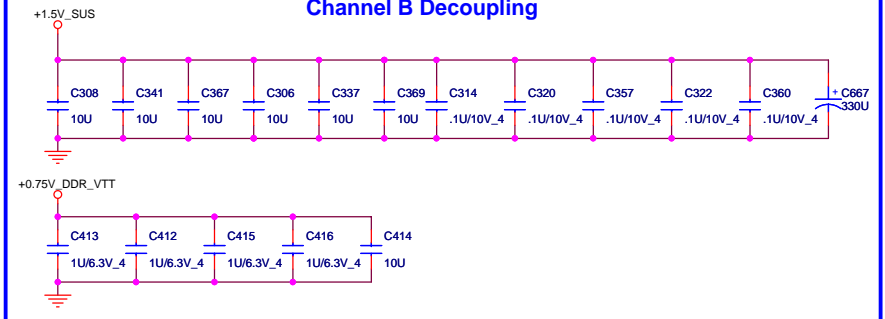
Title			DDR3 DIMM-A
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5/13: Change connector from Tyco to Foxconn to avoid shortage

Channel B



Channel B Decoupling



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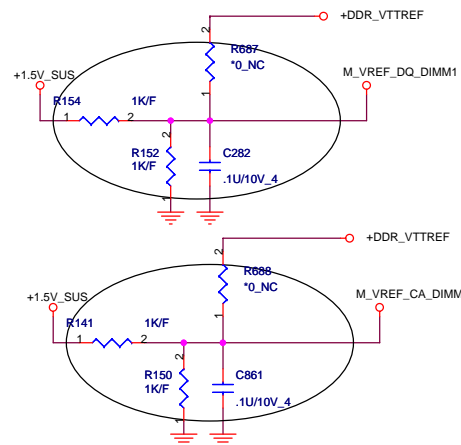
For CH B SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

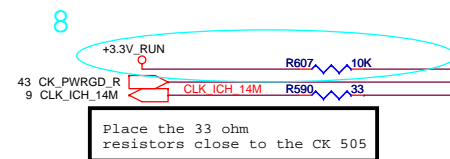
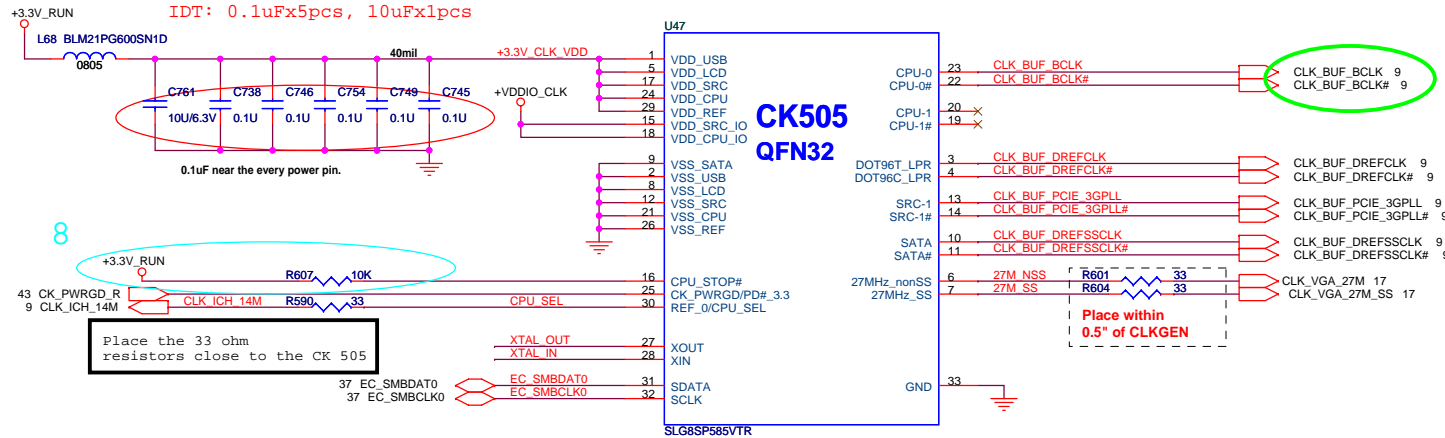
5/18: Separate voltage divider for M_VREF_DQ_DIMM1 and M_VREF_CA_DIMM1 to follow Intel CRB design

6/02: Change M1 from voltage regulator to voltage divider



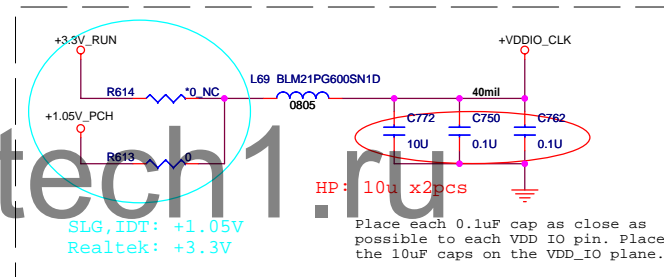
Title			
DDR3 DIMM-B			
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Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs

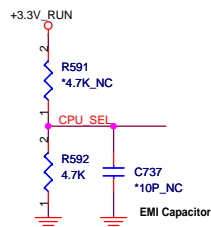


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Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V;
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V;
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.

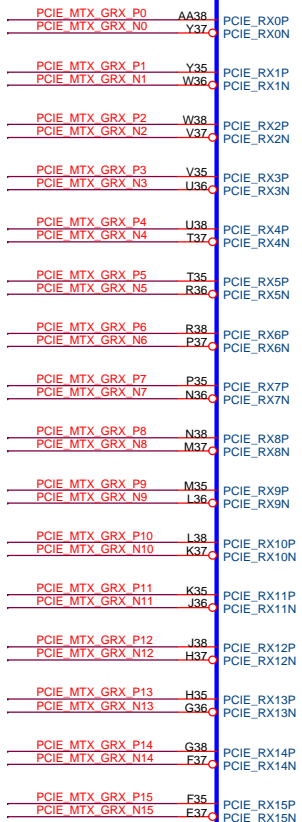


PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V-1.5V)		100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V;
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V;
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V;



3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]



U29A

PCI EXPRESS INTERFACE

ASIC PN 100-CK QCI P/N

M96-M2 XT A13 216-0729051 100-CK3186 AJ072900T08
M97-M2 LP A11 216-0731001 100-CG1806 AJ073100T01

PCIE_MRX_GTX_P[0..15] 3
PCIE_MRX_GTX_N[0..15] 3



9 CLK_PCIE_VGA#
9 CLK_PCIE_VGA#

!!! Park, Madison : Pop 0 Ohm
M96: depop 0 ohm

R426 0 NC

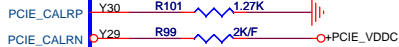
3,9,26,28,29,31,32,41,56 PLTRST#

R100 0 PERST#

0928:QT 0ohm resistor costdown

216-0729051(M96-M2 XT)

CALIBRATION



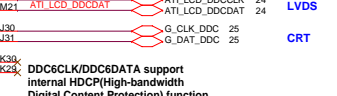
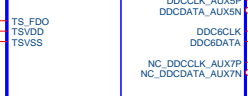
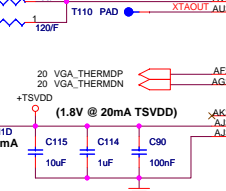
Title M96XT_PCIE		
Size RMSB	Document Number	Rev 3B
Date: Thursday, October 01, 2009	Sheet 16	of 61

Note : Required Frequency = 800 MHz

+3.3V_DELAY



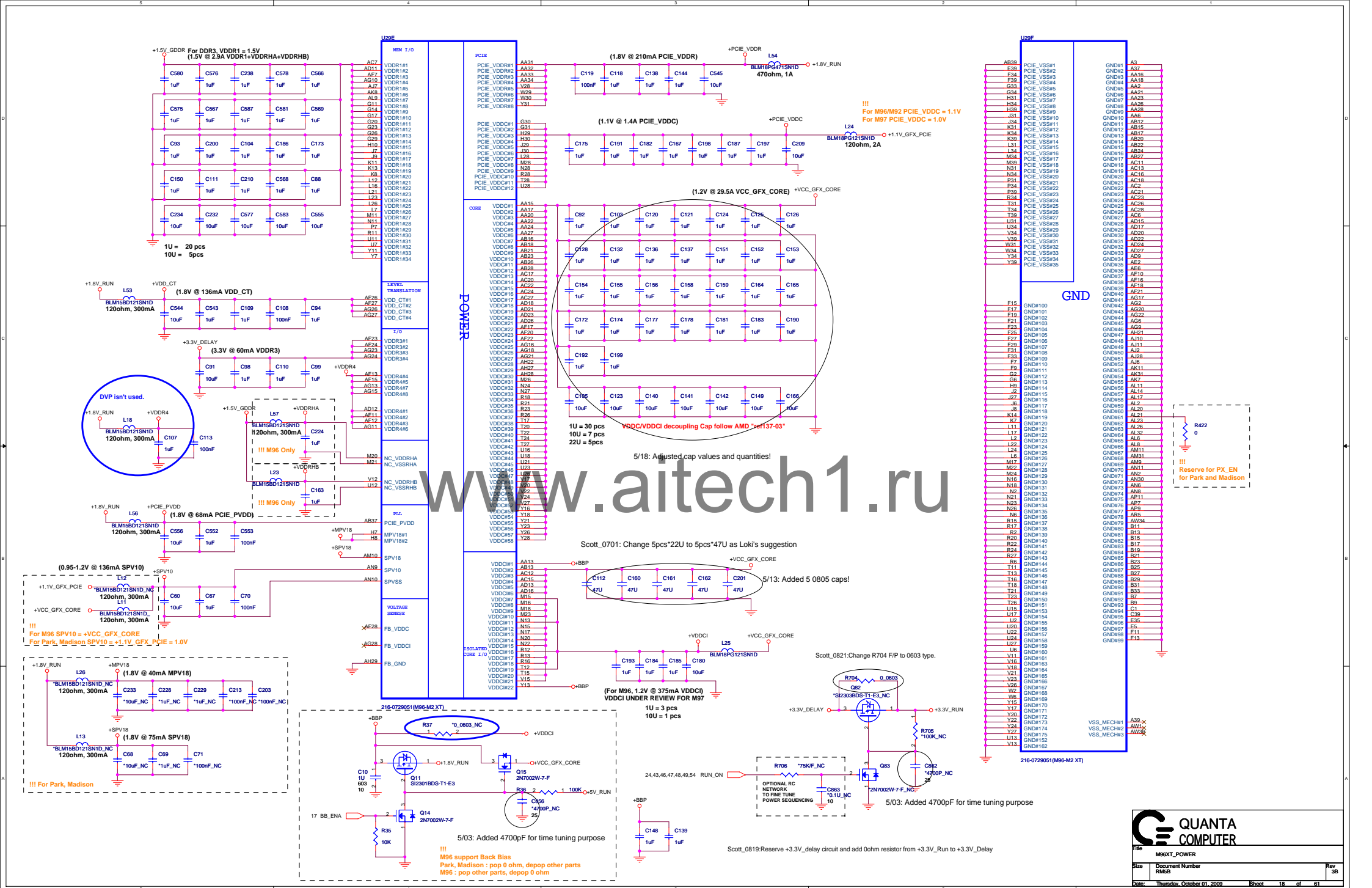
MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0



CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capable enabled The device will not be recognized as the system's VGA controller.	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAAVSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0



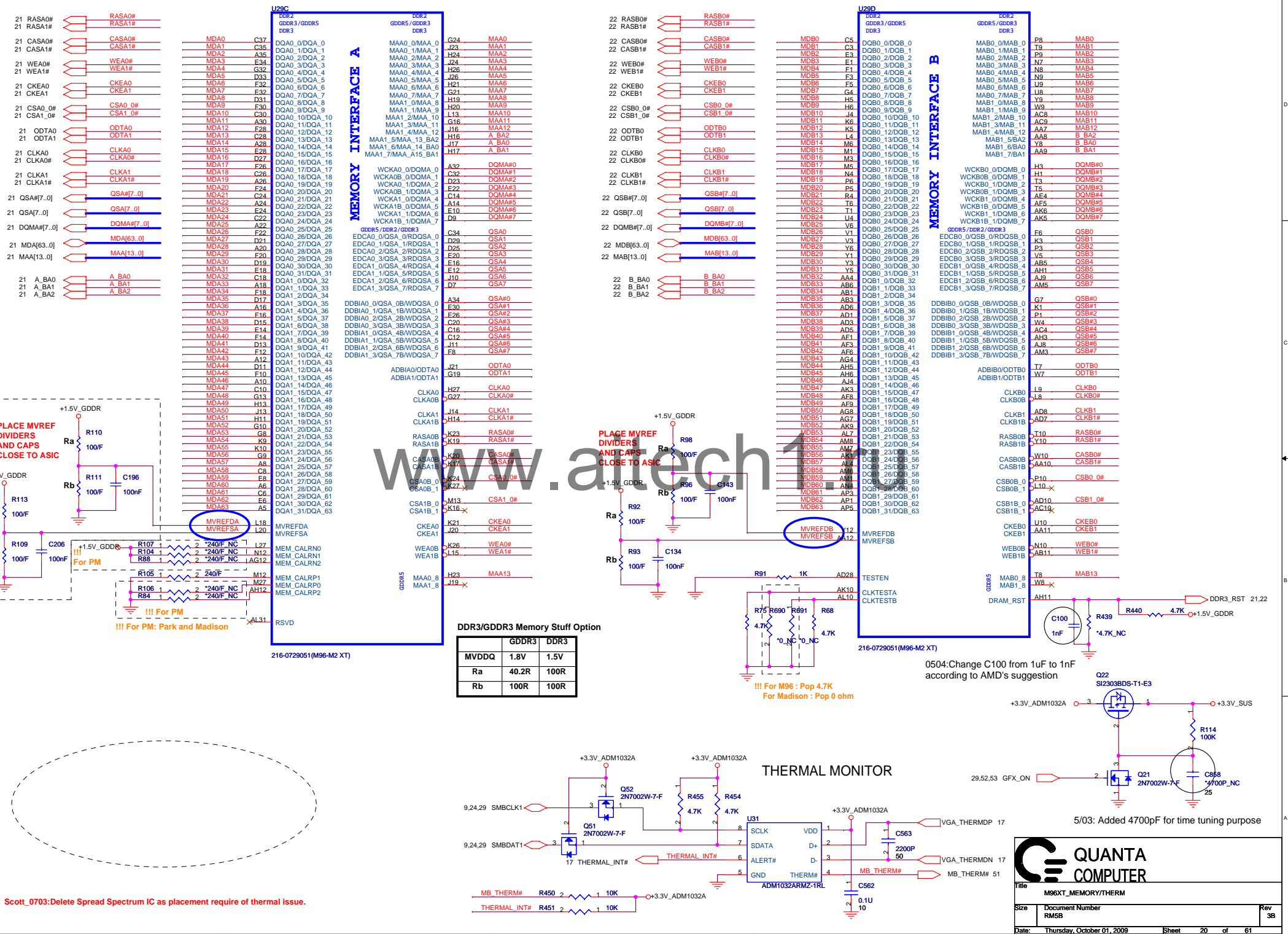
M96XT_IO & STRAP



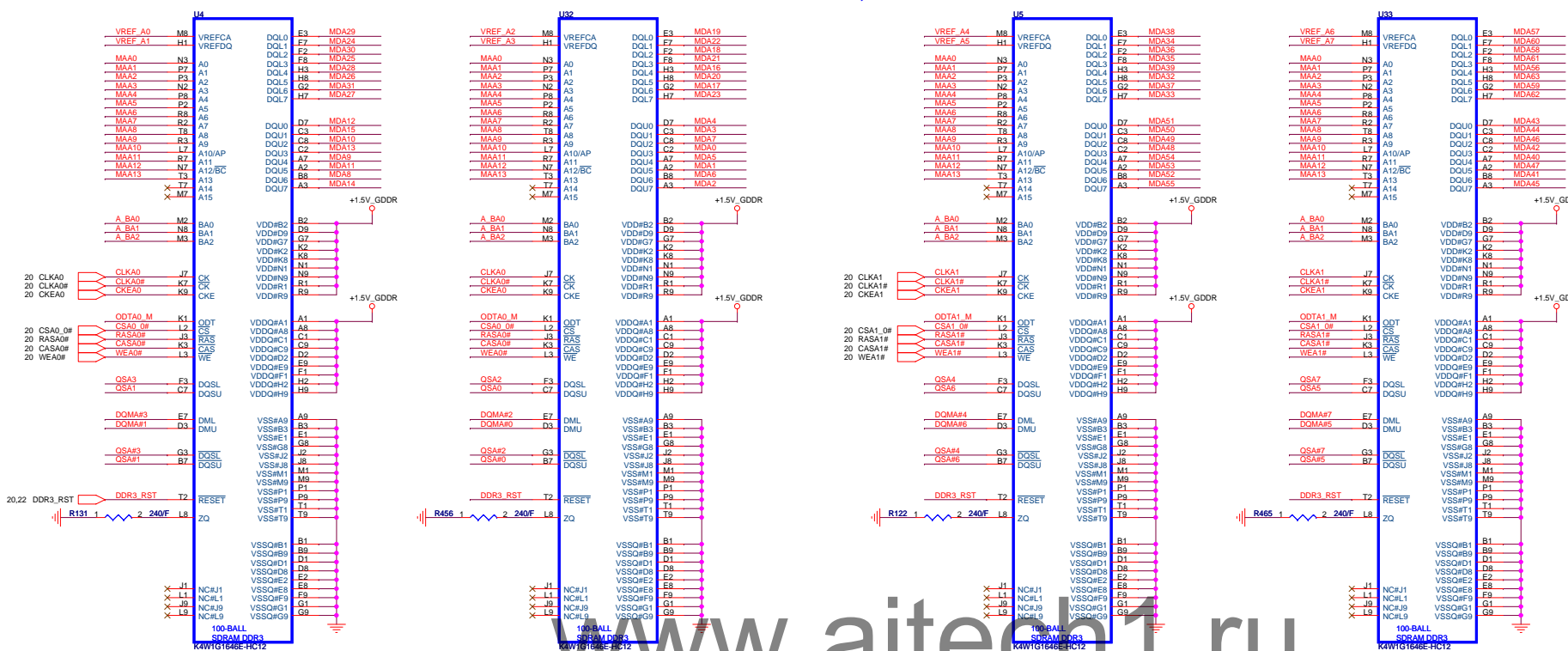
DPC & DPD aren't used.



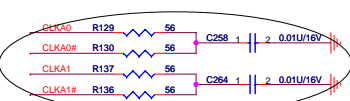
DPA_PVDD)



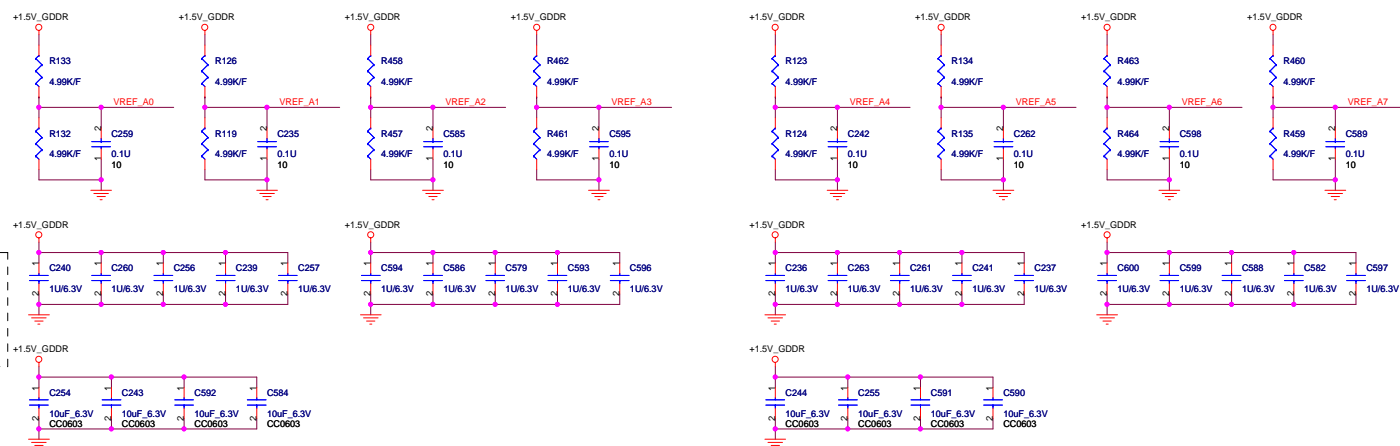
DDR3 64MX16, CH A : 512MB



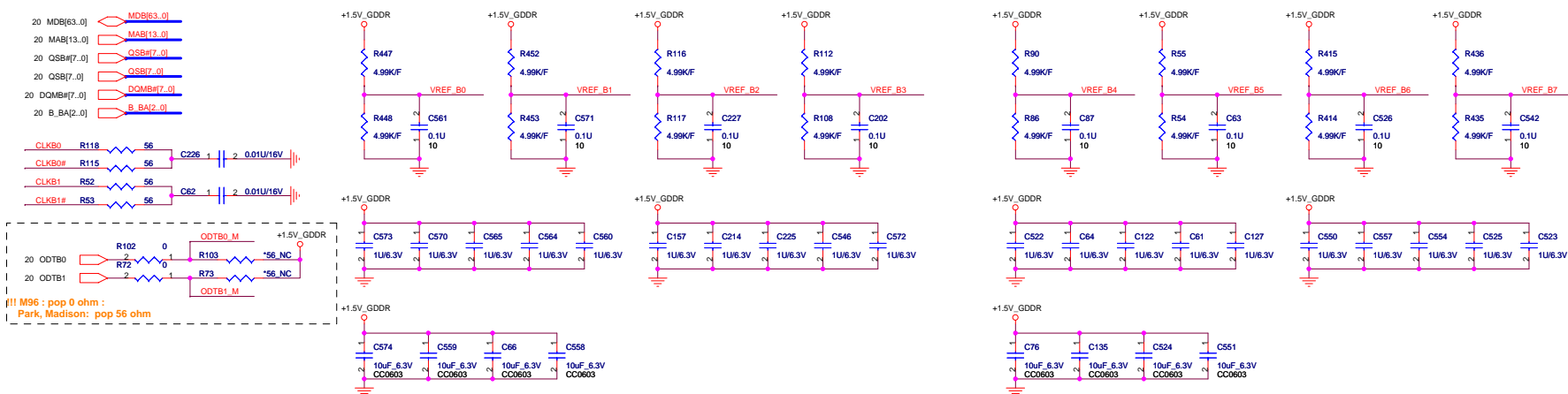
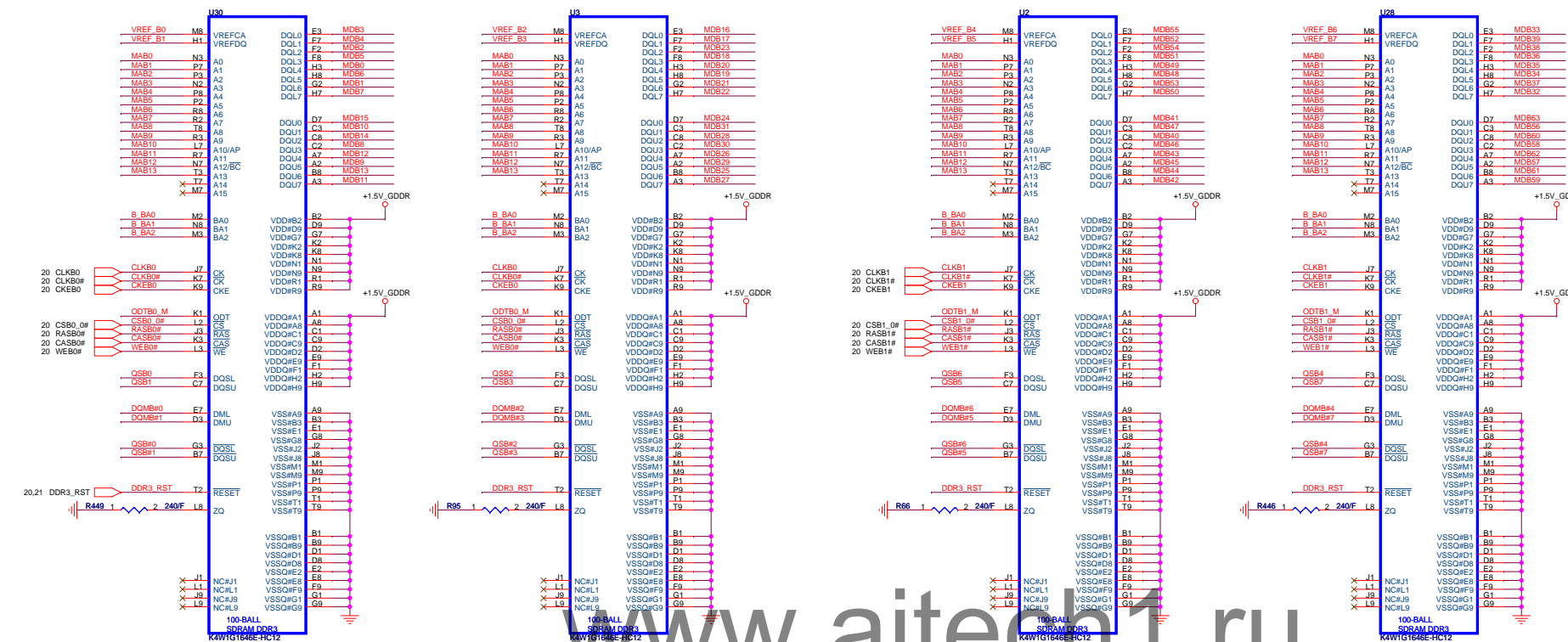
Placement has to be close to VRAM

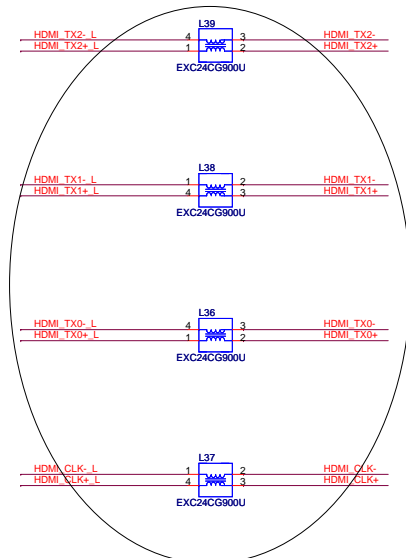
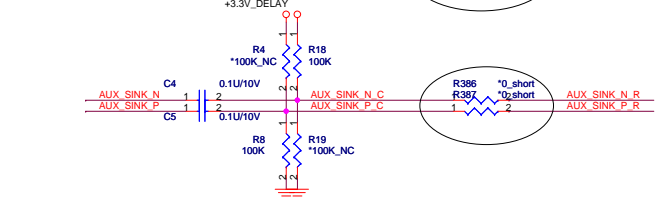
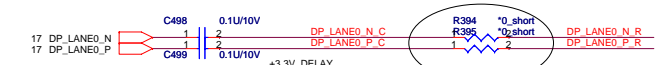
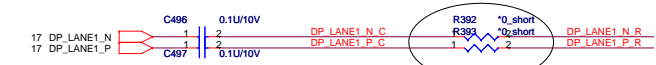
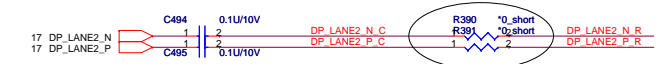
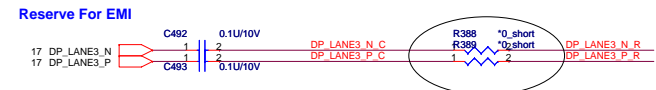
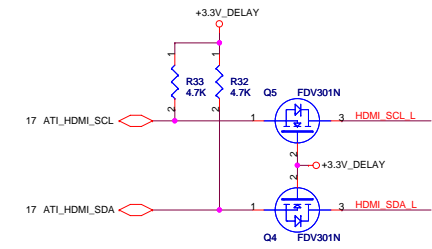
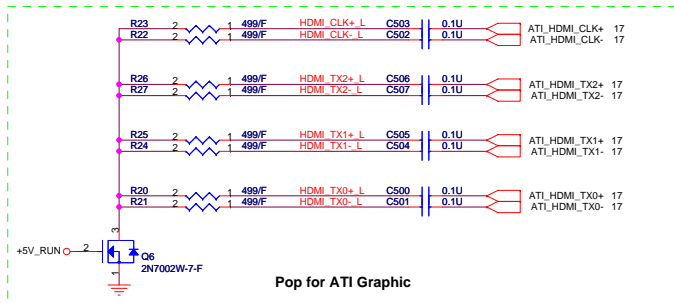


!!! M96 : pop 0 ohm :
Park, Madison: pop 56 ohm



DDR3 64MX16, CH B : 512MB





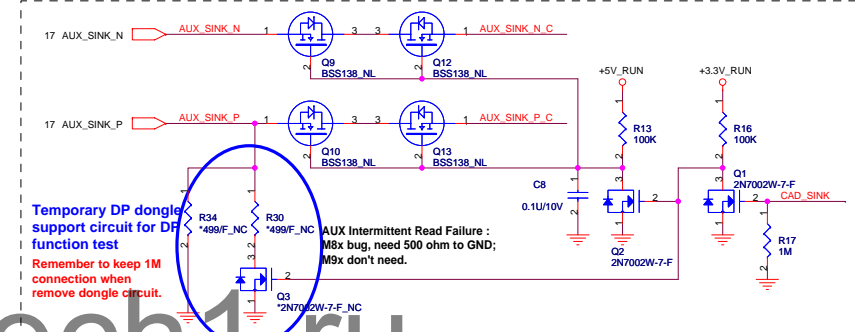
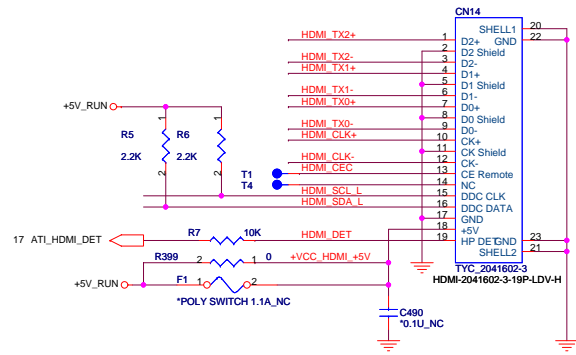
Scott_0814:Delete 0ohm reserve resistors as confirm with EMI.

Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.

Scott_0814:Delete reserve choke as confirm with EMI.

0928:QT 0ohm resistor costdown <R386~R395>

Scott_0703:Delete ESD Clamp U23,U24,U25 as EMI suggestion.



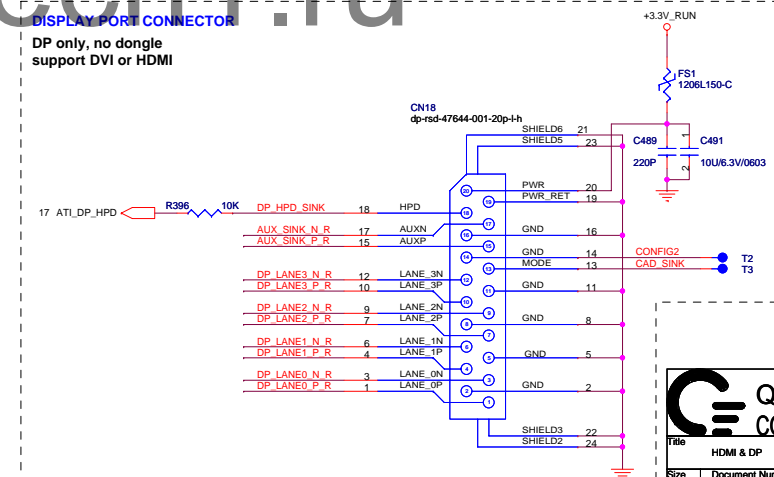
Temporary DP dongle support circuit for DP function test

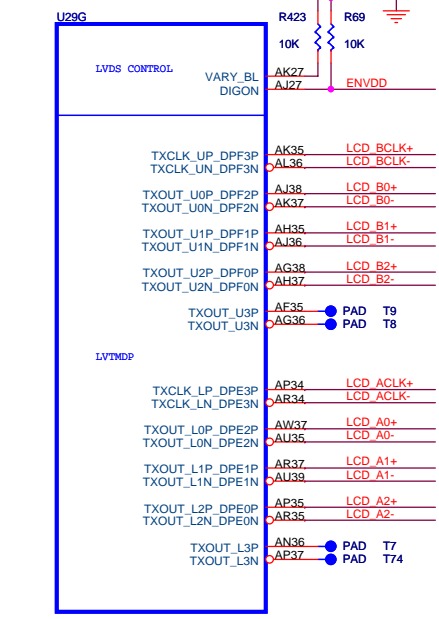
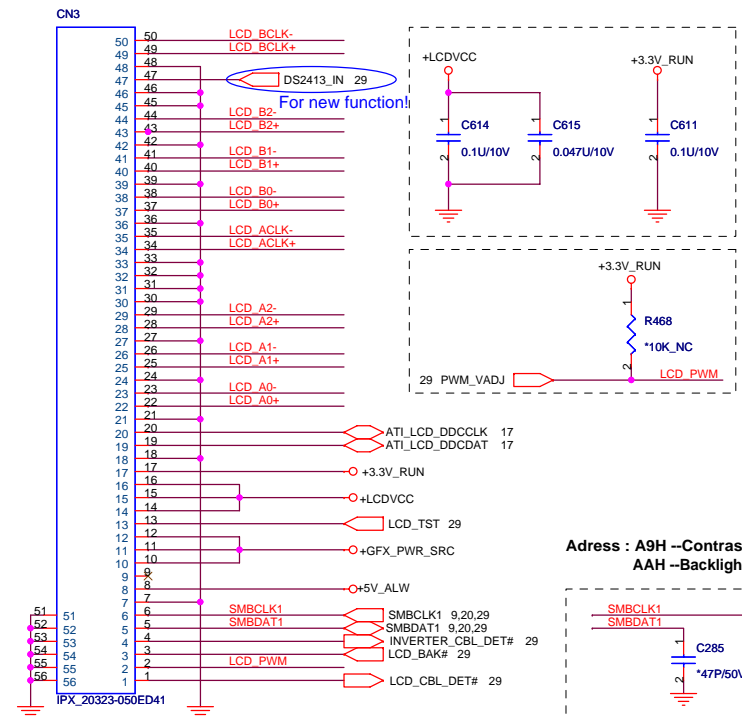
Remember to keep 1M connection when remove dongle circuit.

AUX Intermittent Read Failure : M8x bug, need 500 ohm to GND; M9x don't need.

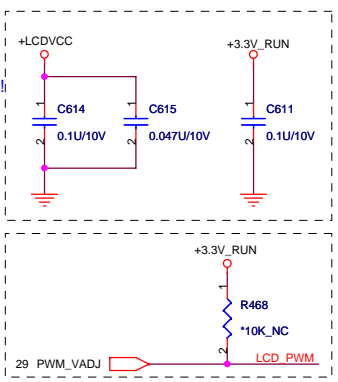
DISPLAY PORT CONNECTOR

DP only, no dongle support DVI or HDMI

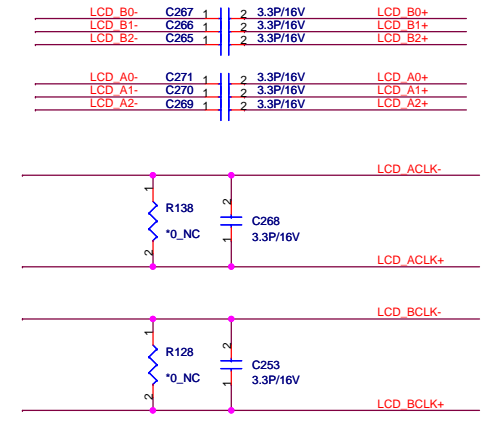




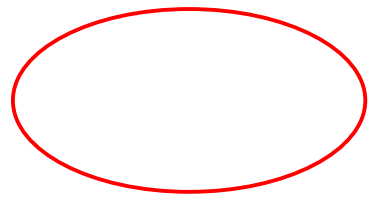
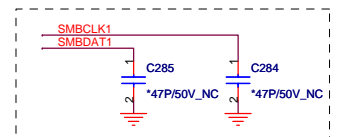
216-0729051 (M96-M2 XT)



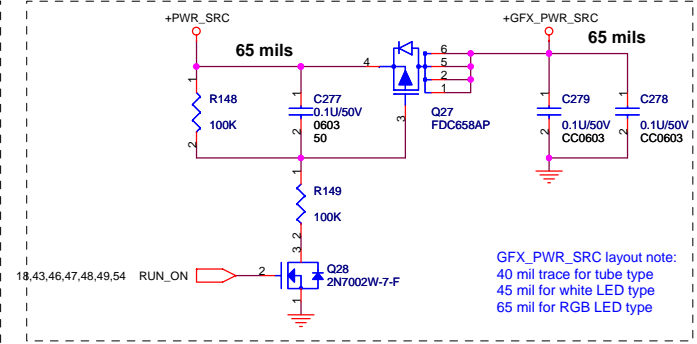
Shunt capacitors on LVDS for improving WWAN.



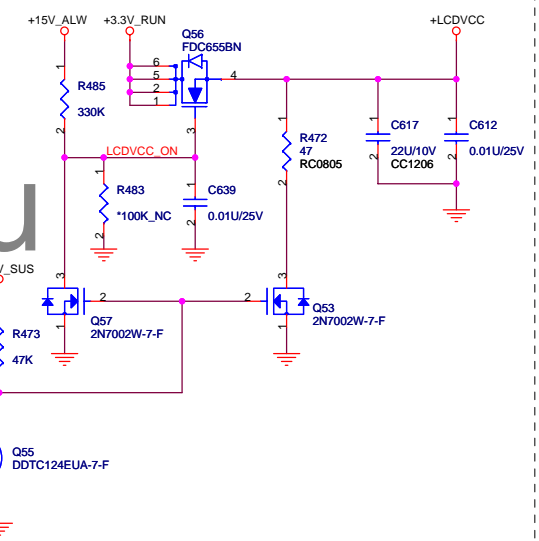
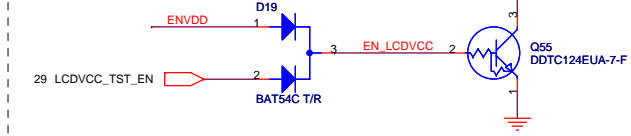
Address : A9H --Contrast
AAH --Backlight

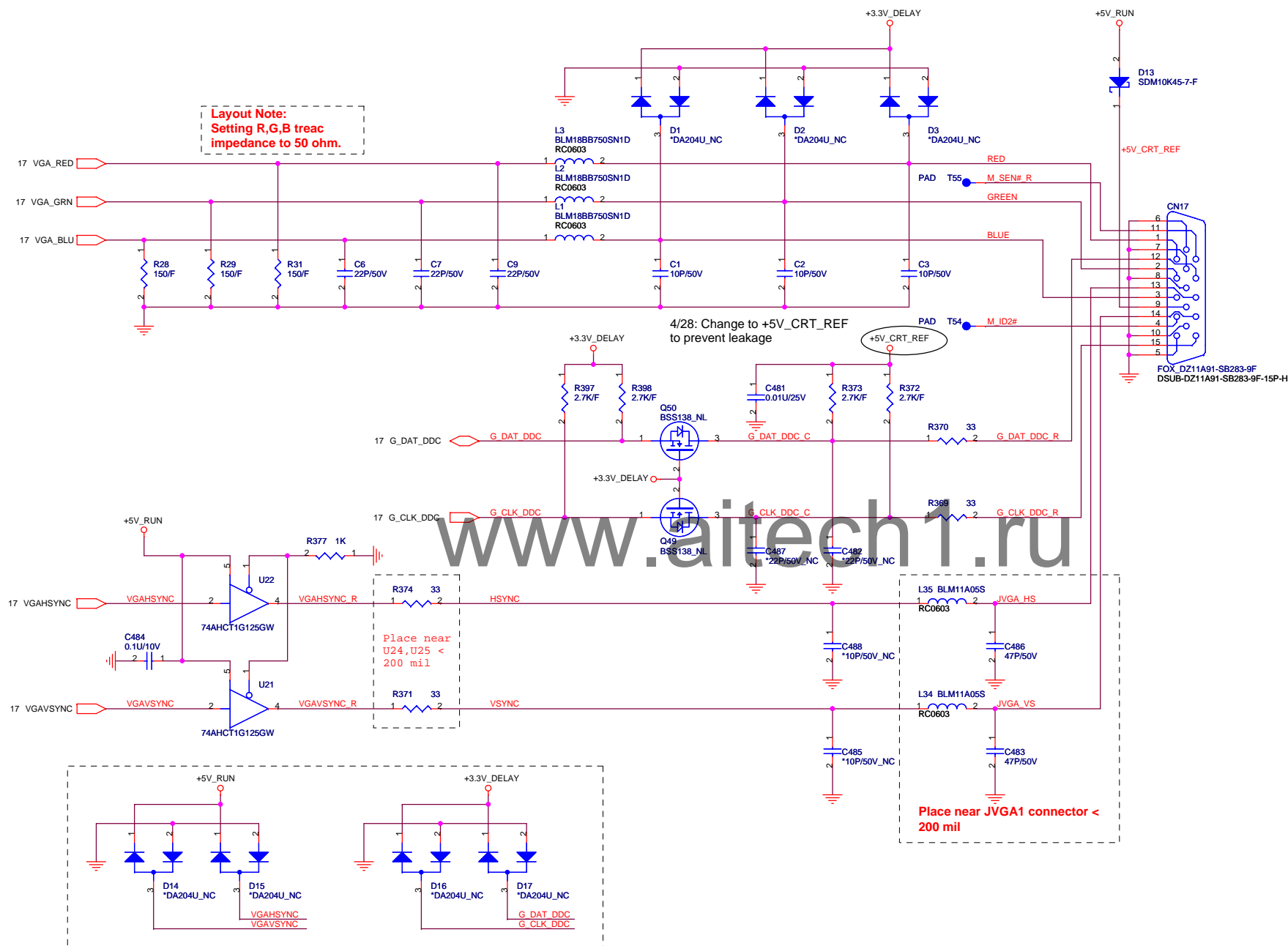


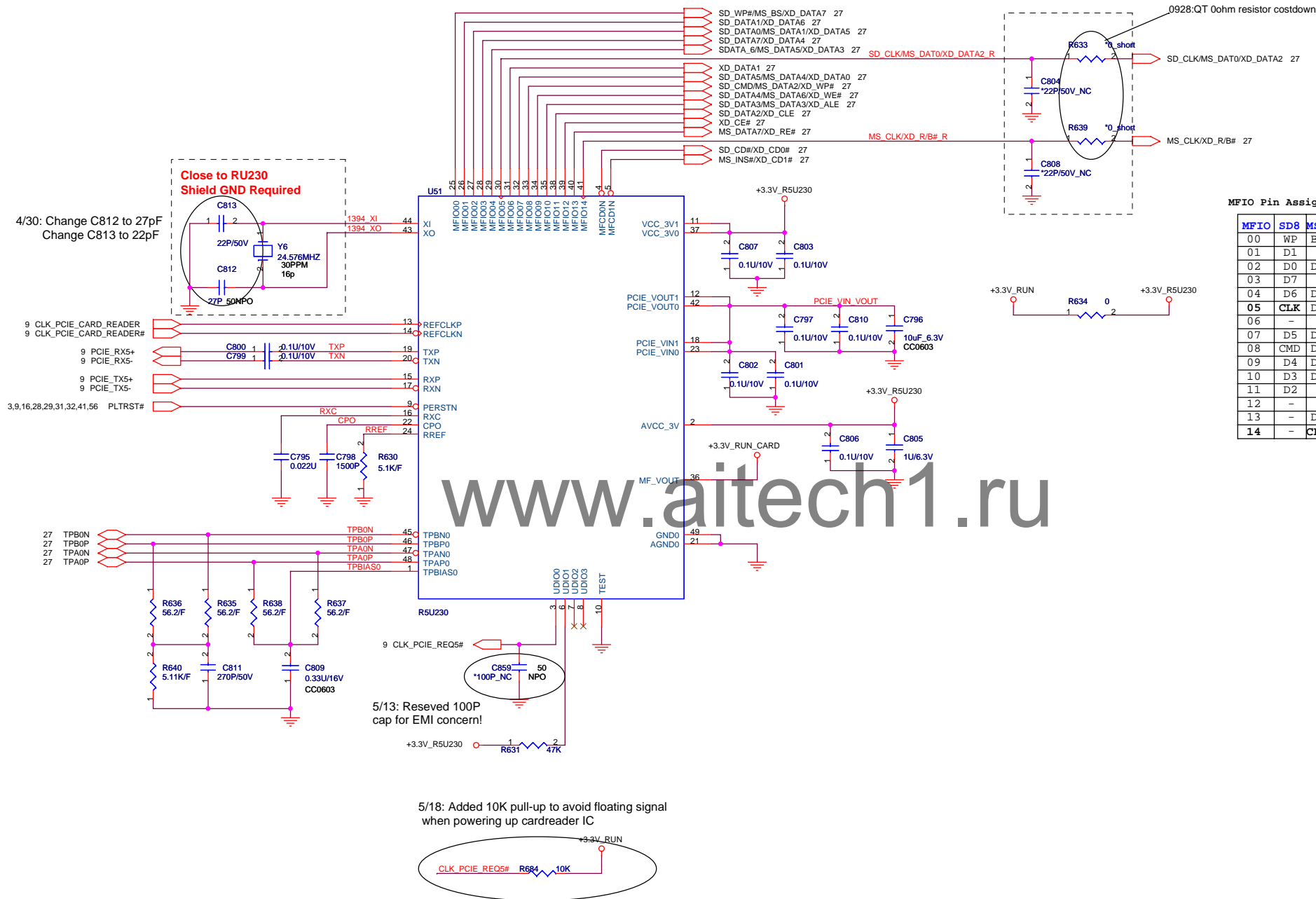
Scott_0812: Delete DPST function as non-used.



Support the new imbedded diagnostics.







MFIO Pin Assignment Table

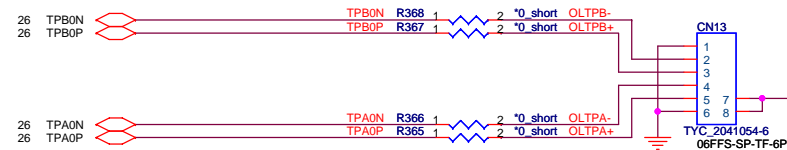
MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#



Title CardReader (5C833)		
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Reserved EMI Solution

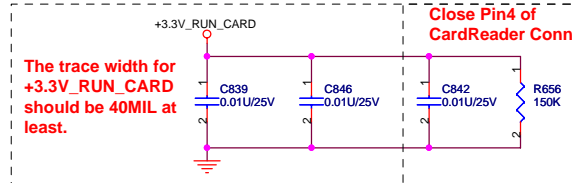
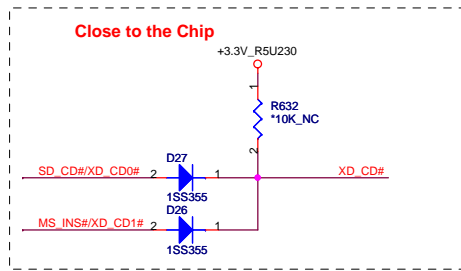
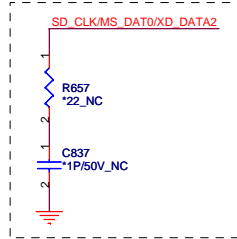
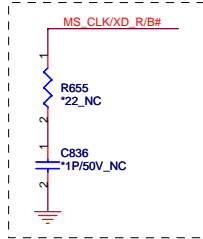
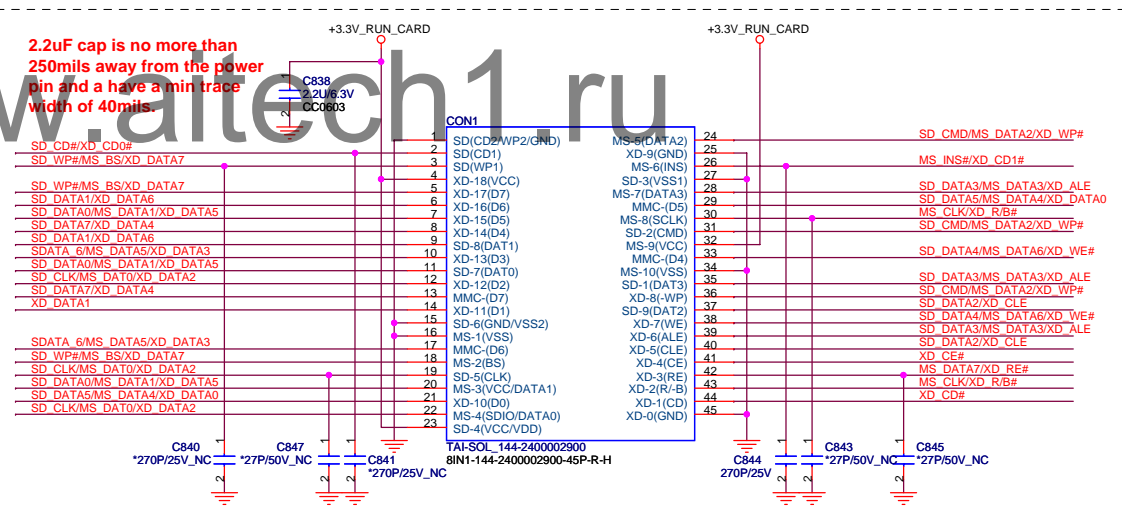
1. TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
2. TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
3. Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



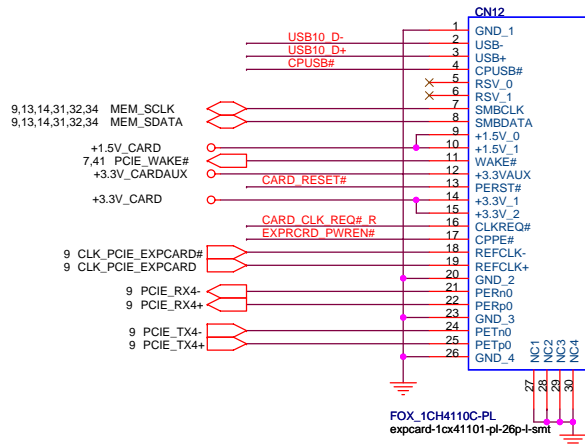
26 SD_WP#/MS_BS/XD_DATA7
26 SD_DATA1/XD_DATA6
26 SD_DATA0/MS_DATA1/XD_DATA5
26 SD_DATA7/XD_DATA4
26 SDATA_6/MS_DATA5/XD_DATA3
26 SD_CLK/MS_DATA0/XD_DATA2
26 XD_DATA1
26 SD_DATA5/MS_DATA4/XD_DATA0
26 SD_CMD/MS_DATA2/XD_WP#
26 SD_DATA4/MS_DATA6/XD_WE#
26 SD_DATA3/MS_DATA3/XD_ALE
26 SD_DATA2/XD_CLE
26 XD_CE#
26 MS_DATA7/XD_RE#
26 MS_CLK/XD_R/B#
26 SD_CD#/XD_CD0#
26 MS_INS#/XD_CD1#

SD_WP#/MS_BS/XD_DATA7
SD_DATA1/XD_DATA6
SD_DATA0/MS_DATA1/XD_DATA5
SD_DATA7/XD_DATA4
SDATA_6/MS_DATA5/XD_DATA3
SD_CLK/MS_DATA0/XD_DATA2
XD_DATA1
SD_DATA5/MS_DATA4/XD_DATA0
SD_CMD/MS_DATA2/XD_WP#
SD_DATA4/MS_DATA6/XD_WE#
SD_DATA3/MS_DATA3/XD_ALE
SD_DATA2/XD_CLE
XD_CE#
MS_DATA7/XD_RE#
MS_CLK/XD_R/B#
SD_CD#/XD_CD0#
MS_INS#/XD_CD1#

2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

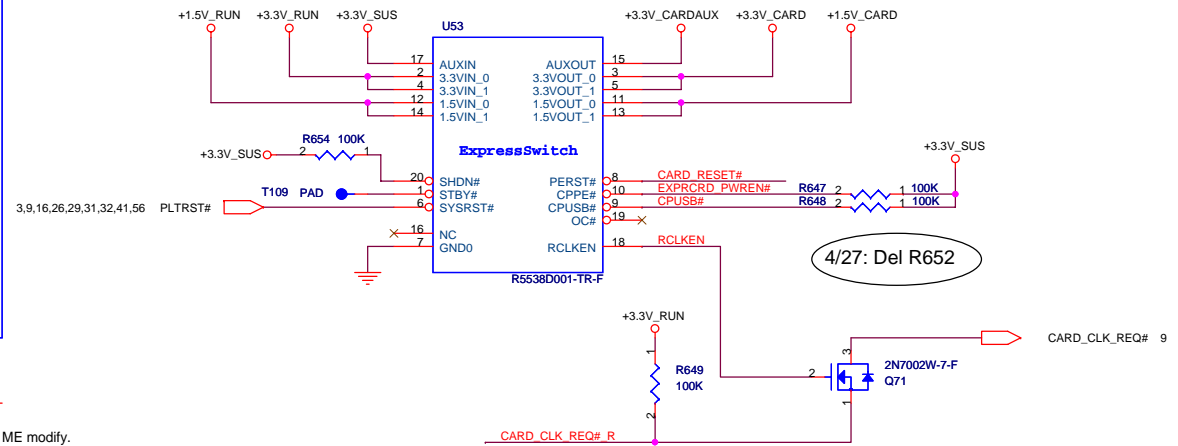


Express Card



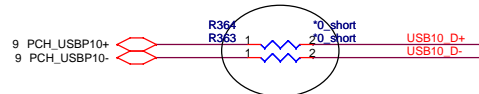
Scott_0813:Change CN12 F/P to expcard-1cx41101-pl-26p-l-smt as ME modify.

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



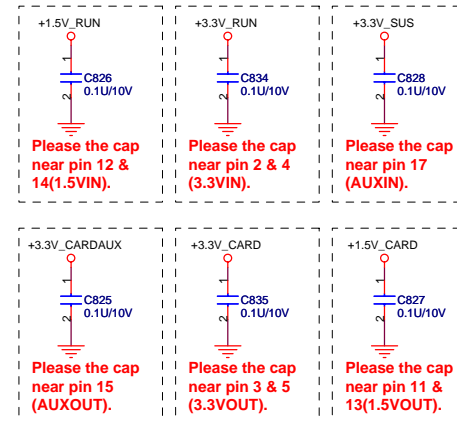
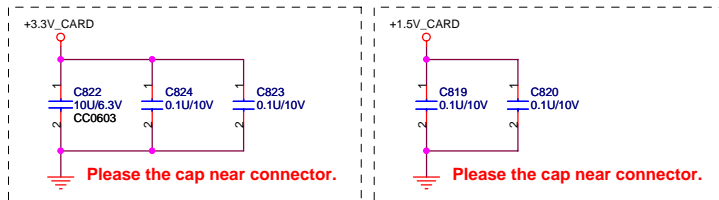
www.aitech1.ru

PCI-Express TX and RX direct to connector.

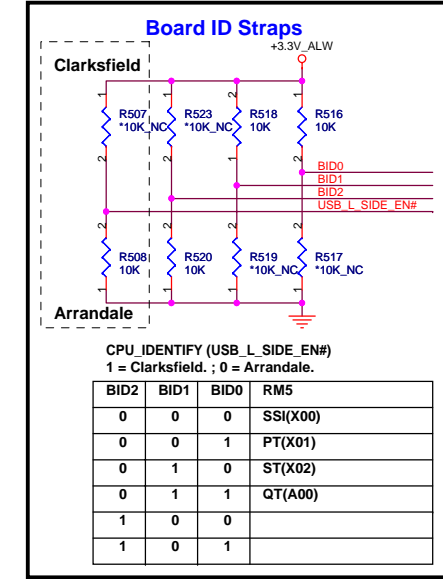


Scott_0814:Delete L31 as confirm with EMI.

0928:QT 0ohm resistor costdown

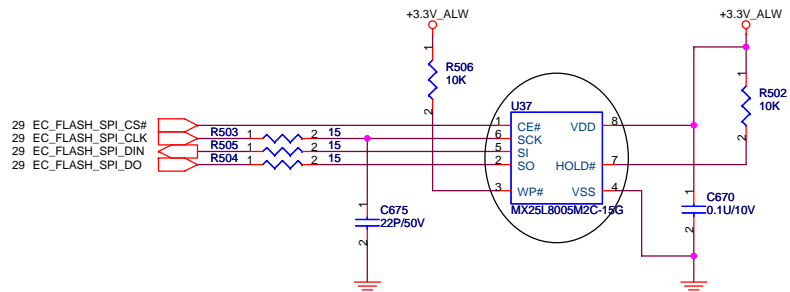


Title EXPRESS CARD		
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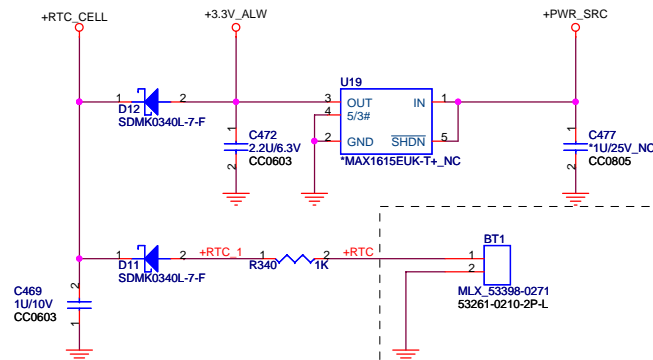


EC SPI ROM, 8Mbit (1M Byte)

5/12: Change U37 from 2MB to 1MB according to BIOS request!

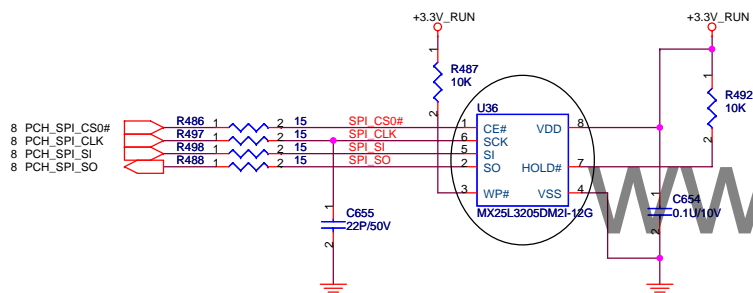


RTC BATTERY

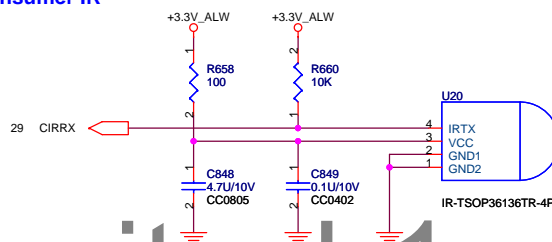


PCH SPI ROM, (4M Byte)

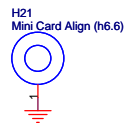
5/12: Change U36 from 2MB to 4MB according to BIOS request!



Consumer IR

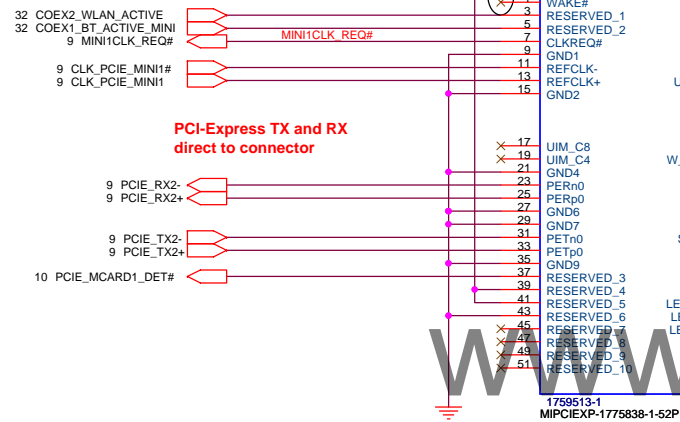


Mini Card Nut



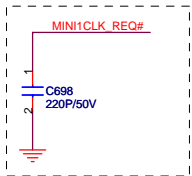
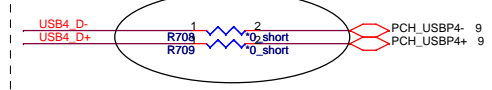
MiniCard WLAN Connector

5/15: Change WAKE# to NC as it is not required



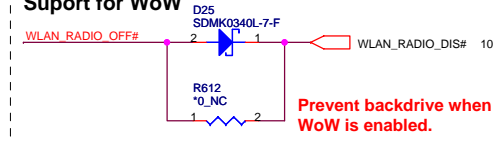
0928:QT 0ohm resistor costdown; 0730: EMI confirm remove L70

Reserved PAD for EMI

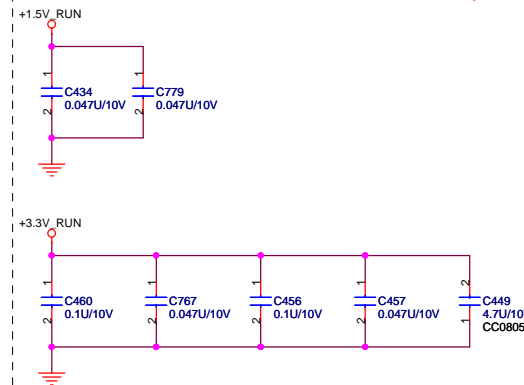


5/03: Added 100p to PLTRST# and PCIE_WAKE# according to EMI request

Support for WoW



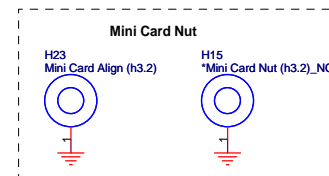
Place caps close to connector.



Title MINI-CARD (WLAN)		
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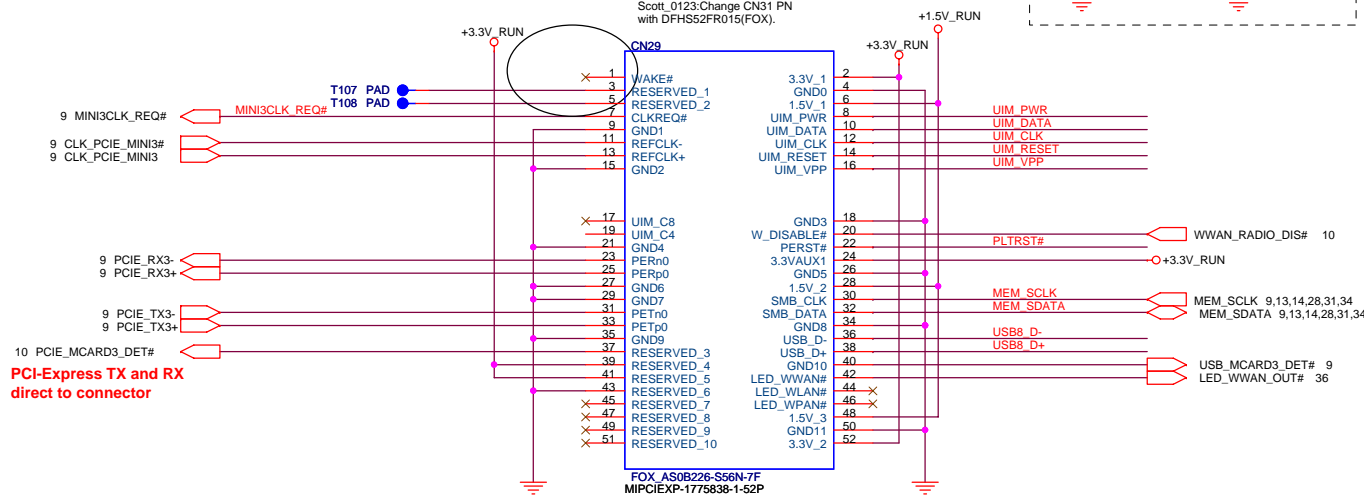
5/15: Change WAKE# to NC as it is not required

MiniCard WWAN Connector

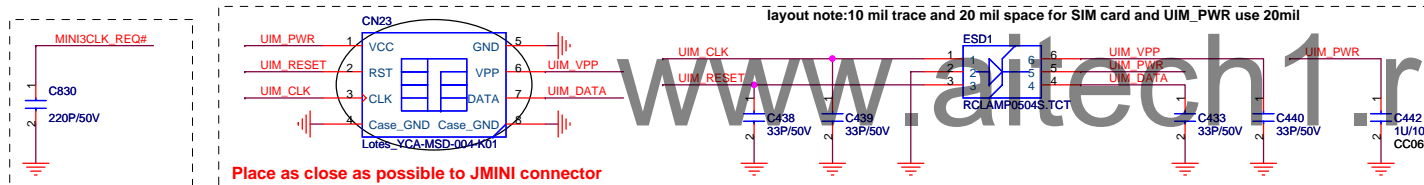


USB8 D- 1 R710 2 *0_short PCH_USB8- 9
 USB8 D+ 1 R711 2 *0_short PCH_USB8+ 9

Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

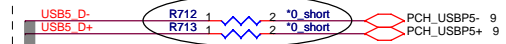


5/13: Change SIM card connector to Lotes



layout note:10 mil trace and 20 mil space for SIM card and UIM_PWR use 20mil

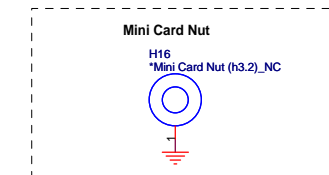
Reserve For EMI



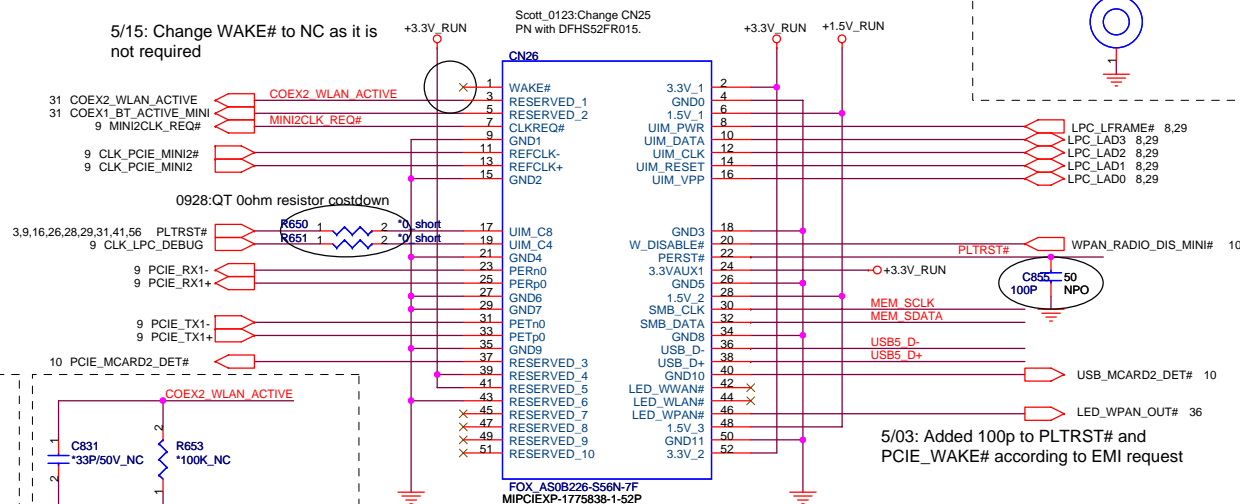
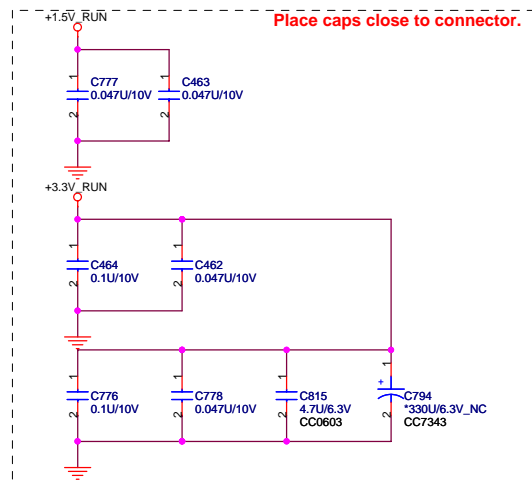
Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

MiniCard Robson, BT. UWB Connector

X2_WLAN_ACTIVE COEX2 WLAN ACT



Mini Card Nut
H16
*Mini Card Nut (h3.2)_NC



5/03: Added 100p to PLTRST# and
PCIE_WAKE# according to EMI request



Title			
MINI-CARD (WPAN,WWAN)			
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[illegible]

5/11: Reserved 0 ohms for
Pericom enhanced mode select
5/12: Change IC to Pericom
as Maxim failed EA test
6/23: NC according to Pericom
reccomandation!

Each channel is 1A

29 USB_SIN_SIDE_EN#

U15

IN

EN1#

EN2#

OUT1 OC1#

OUT2 OC2#

GND

1

2

3

4

5

6

7

8

C447

0.1uF/50V

CC0603

TPS2062DR

OC1# 9

Place one 150uF cap by each USB connector.

The schematic diagram illustrates the USB2 to RS485 converter circuit. The circuit includes a MAX4983EEVB+ IC (U17) which serves as the bridge between the USB and RS485 interfaces. The power supply is provided by +5V_ALW and +USB_RIGHT_PWR. The RS485 interface is connected to a 485 module with COM1, COM2, and EN pins. The USB interface is connected to a USB module with D+ and D- pins. The bridge IC (U17) has pins NC1, NC2, NO1, NO2, and CB. The voltage divider consists of resistors R355 (75K_F), R353 (43.2K_F), R625 (49.9K_F), and R624 (49.9K_F). A capacitor C468 (0.1U/10V) is connected to the +5V_ALW supply.

CN16
 MLX_733660490
 mcx-73366-049-5p

CN1
 TYC_1909763-1
 MINIRF-1909763-1-3P

R376
 R3
 R375
 R2

RF_GND

Add a metal cap for TV sensitivity concern. BOM location use PV8, actually mount on PV7, PV8 & PV9.

PV2
 PAD181X67

PV4
 PAD181X67(FBRM2035)

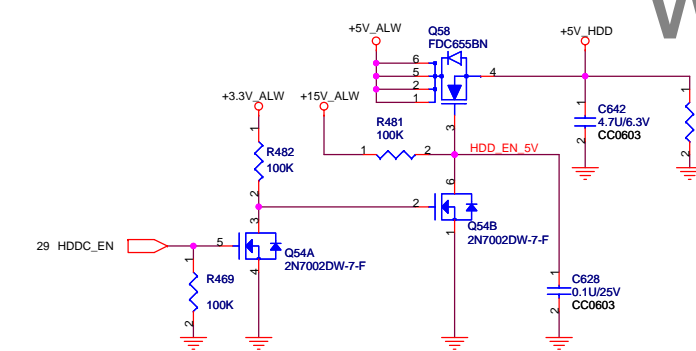
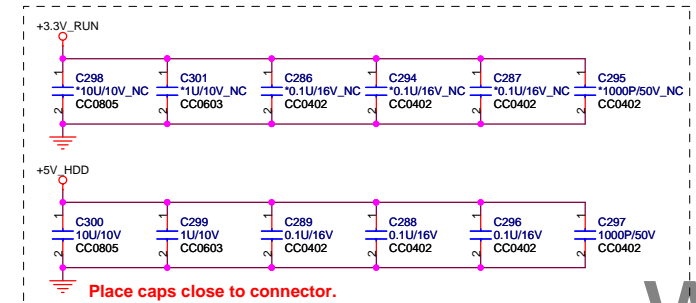
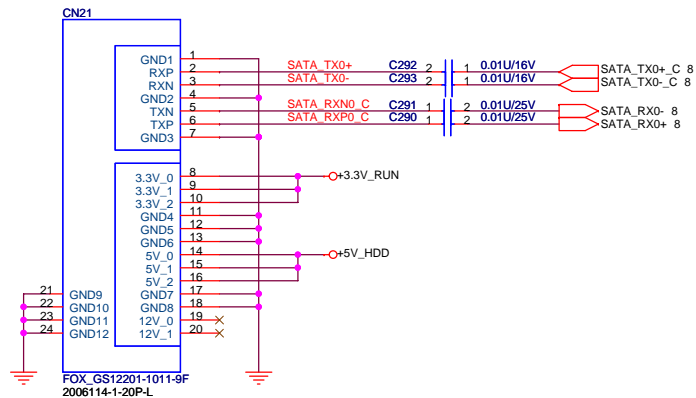
PV3
 PAD18X67

GND

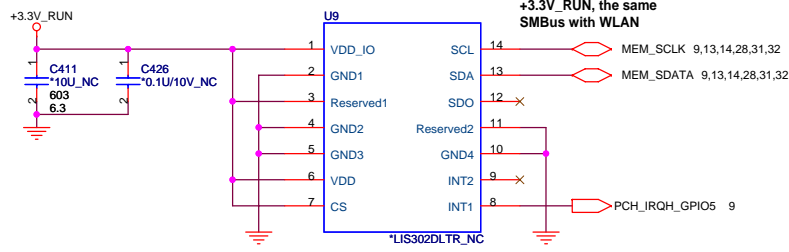
RF_GND

File	USB & eSA
Size	Document 1
	RM5B

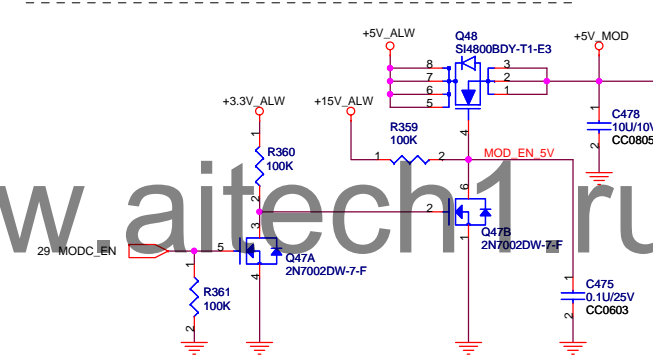
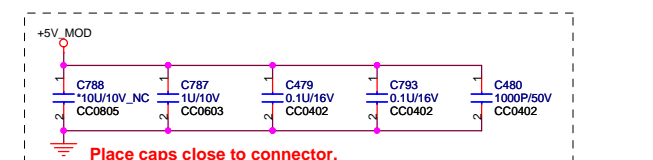
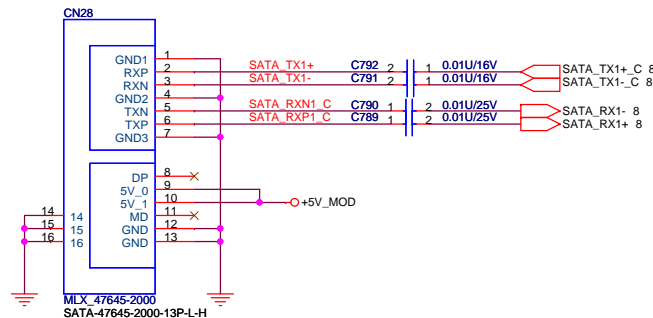
SATA Connector



3-axis Fall Sensor (HDD data protector)



ODD Connector



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HDD & ODD (SATA)		
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To Daughter Board connector

Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White" = System in Standby (S3);

Power Button

Speaker

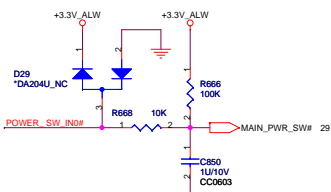
KB LED

Touch Pad

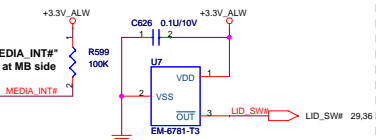
Media Button

Scott_0123:Change CN8 PN with DFHD32MR003(With mylar)

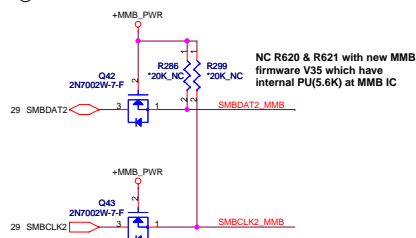
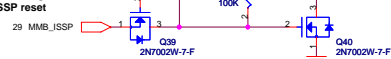
Power Button



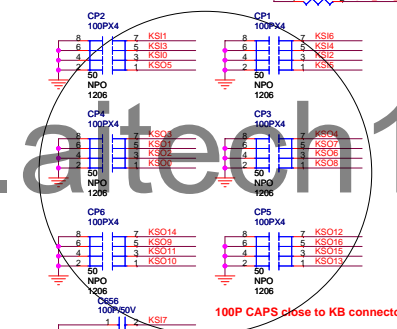
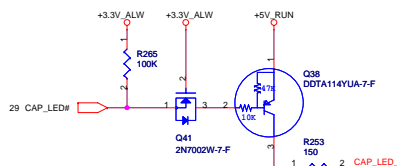
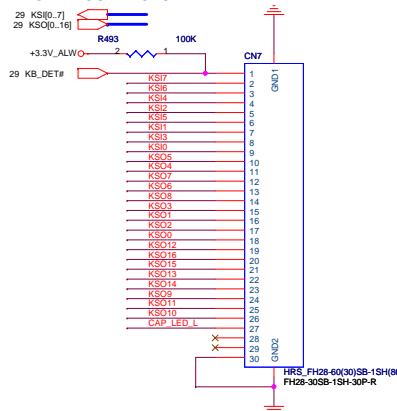
Hall Switch



Active high for ISSP reset



KEYBOARD CONNECTOR



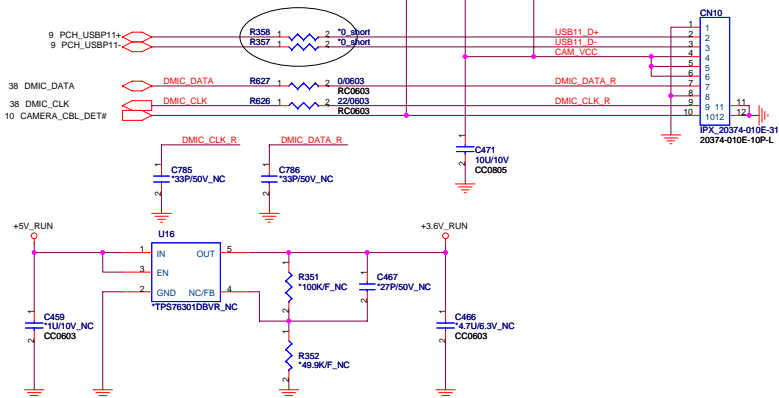
5/03: Populate according to EMI request!

5/12: Change from CA110084N04 to CA110084N39 due to material shortage!

Array Microphone & Camera

Scott_0814:Delete L29 as confirm with EMI.

0928:QT 0ohm resistor costdown



The GND (pin 8) for DMIC is defined as AGND. Connect with GND at MB, but separate AGND & GND at coaxial cable & CCD module.



KB/CCD/ UI

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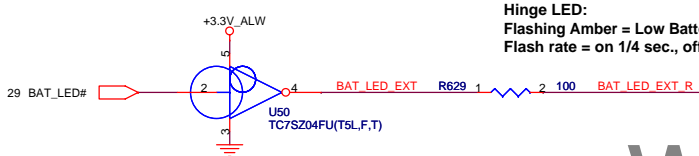
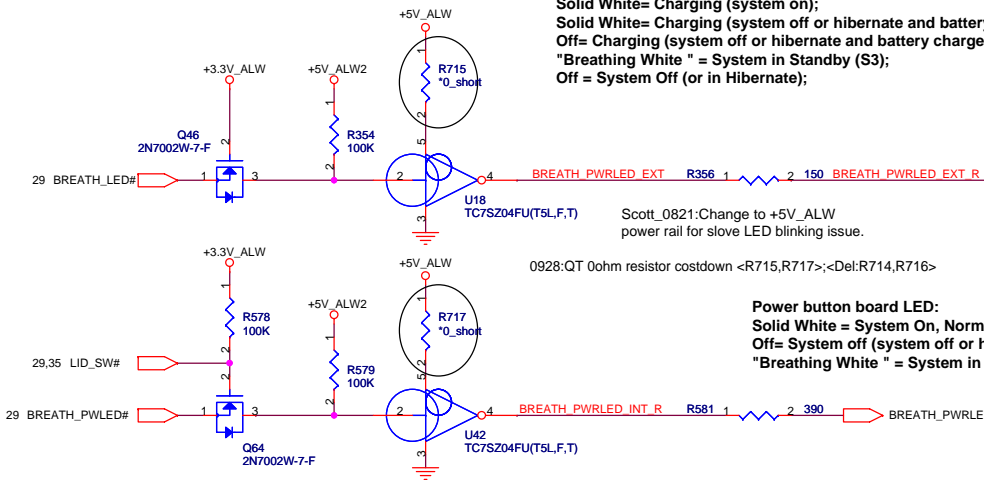
Date: Thursday, October 01, 2009

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Hinge & Power Button board LED (PWR/Battery indicator)

Hinge LED

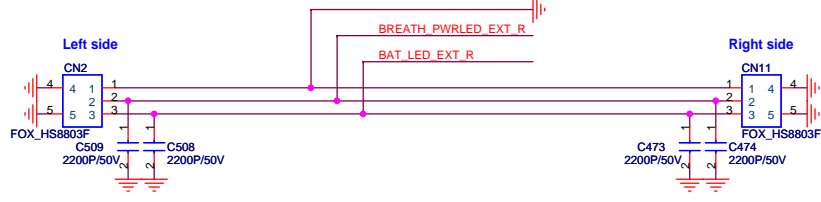
Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);



Hinge LED:
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

Hinge LED (PWR/Battery indicator)

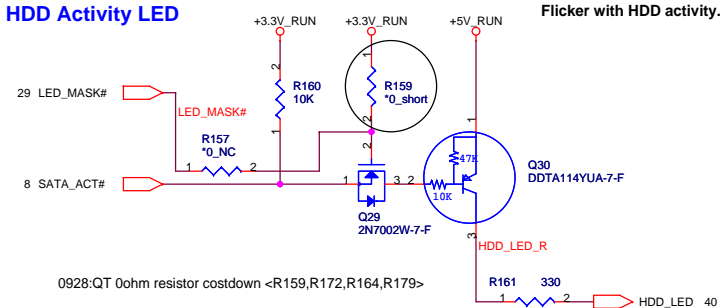
L-C filter (reserve R-C) for EMI



Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

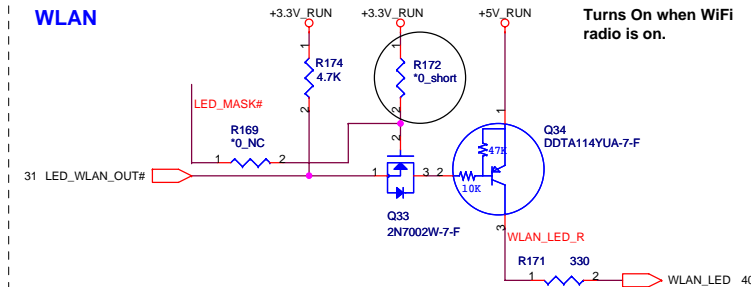
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

HDD Activity LED



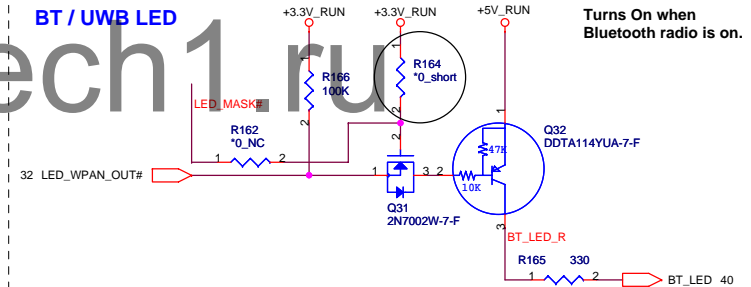
0928:QT 0ohm resistor costdown <R159,R172,R164,R179>

WLAN



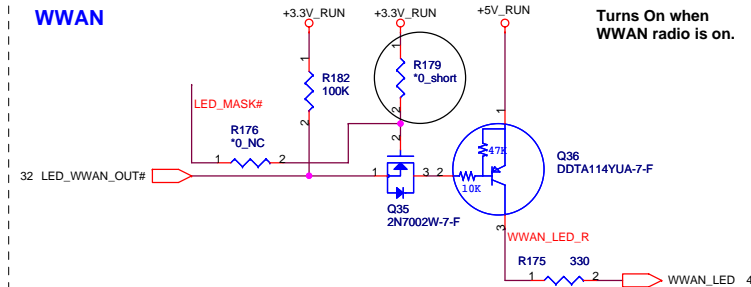
Turns On when WiFi radio is on.

BT / UWB LED



Turns On when Bluetooth radio is on.

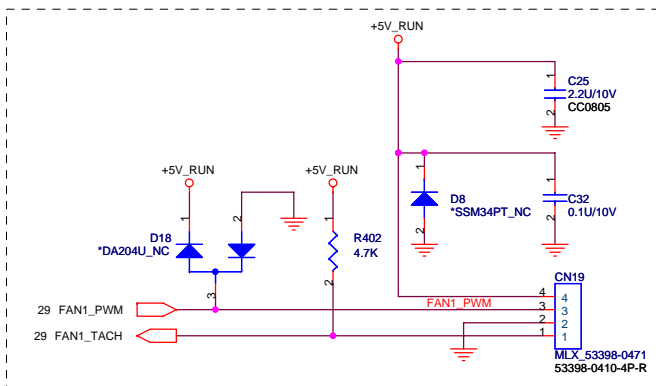
WWAN



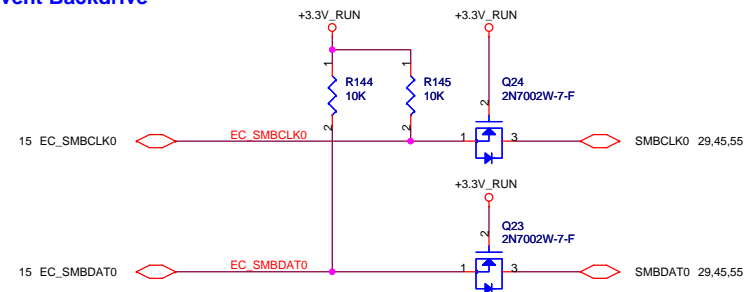
Turns On when WWAN radio is on.



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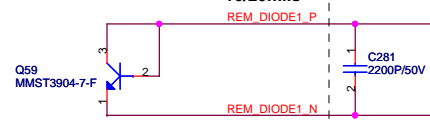


Prevent Backdrive



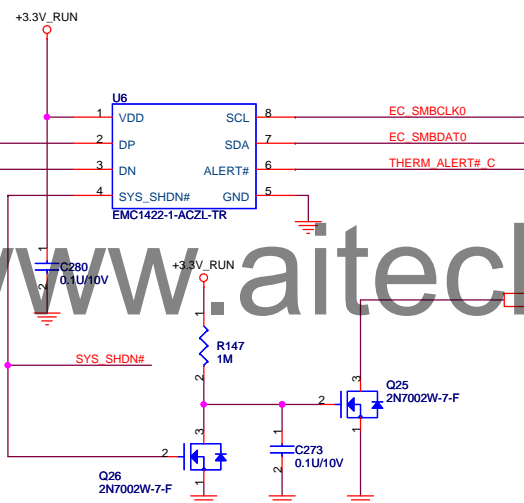
Place these under CPU

10/20mils

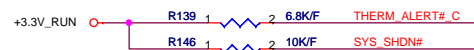


1. Place C579 close to EMC1422
Total capacitance between D+/D- is 2200pF(max)

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OTP 90 degree

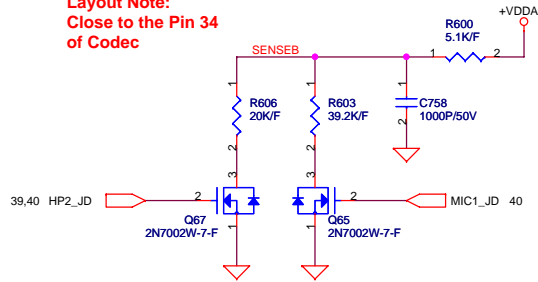


OTP 85 degree : R98 = 10K, R103 = 6.8K
OTP 90 degree : R98 = 6.8K, R103 = 10K

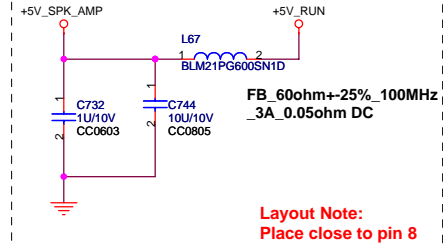
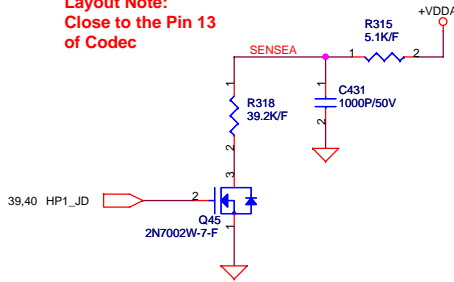


Title			FAN /THERMAL
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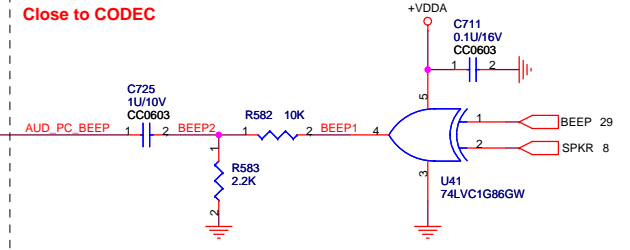
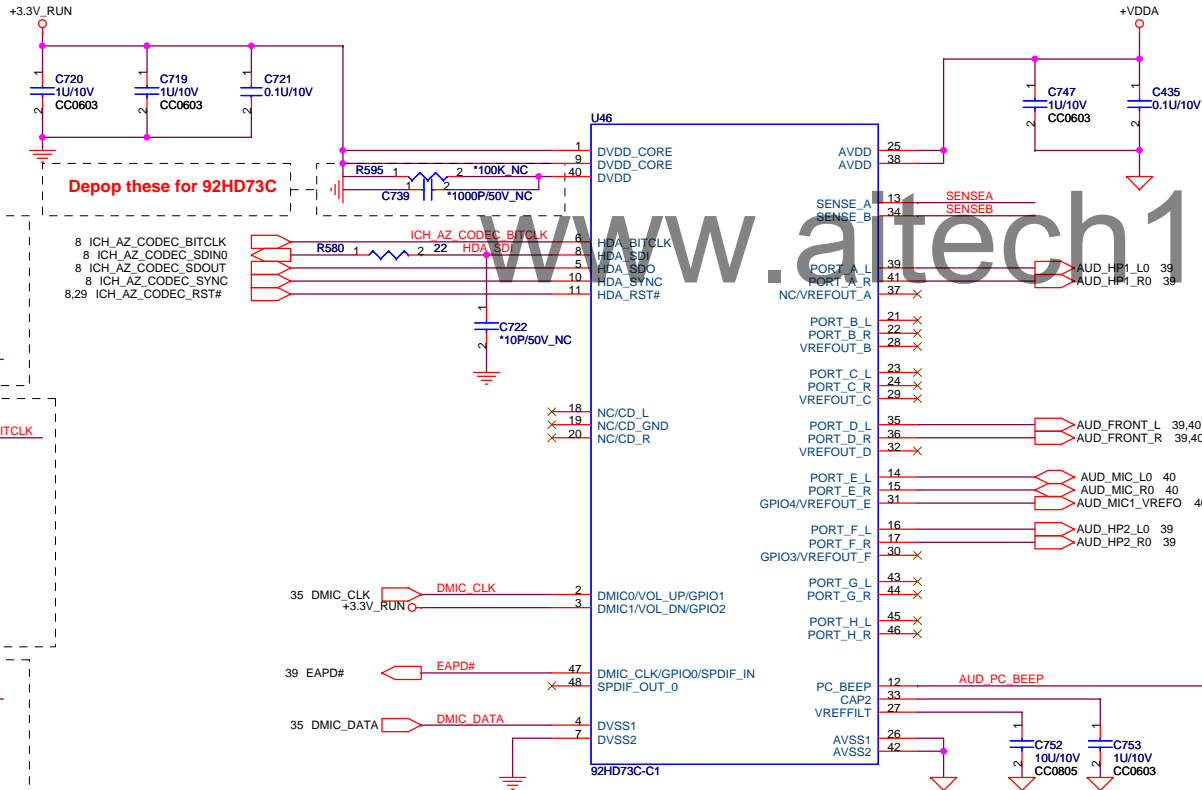
Layout Note:
Close to the Pin 34
of Codec



Layout Note:
Close to the Pin 13
of Codec

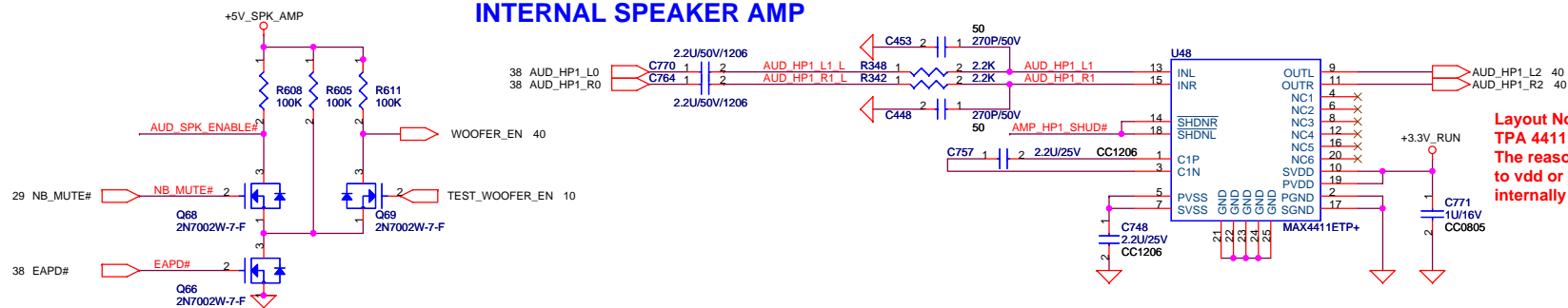


AZALIA (HD) CODEC

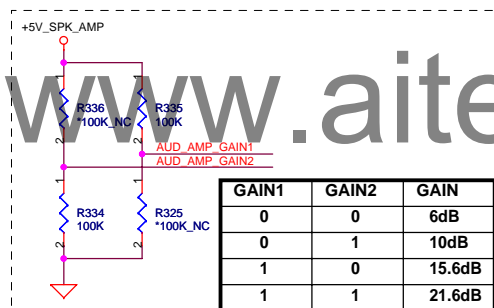
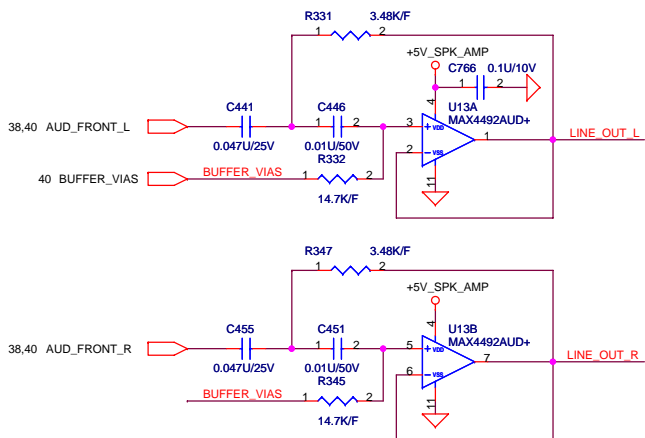
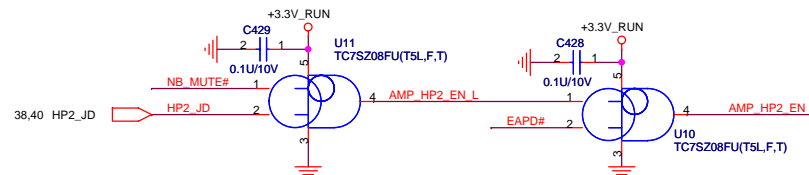
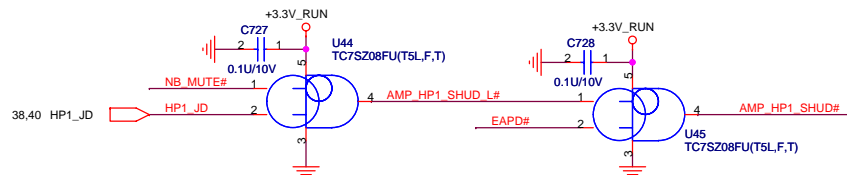


Title			AZALIA CODEC (92HD73C)
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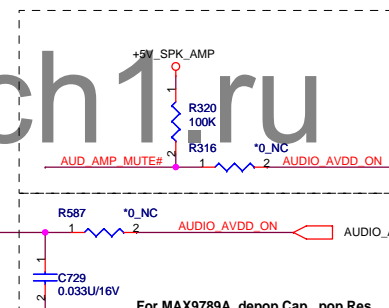
INTERNAL SPEAKER AMP



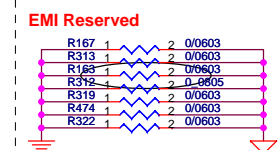
Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



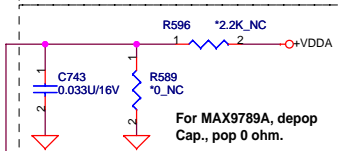
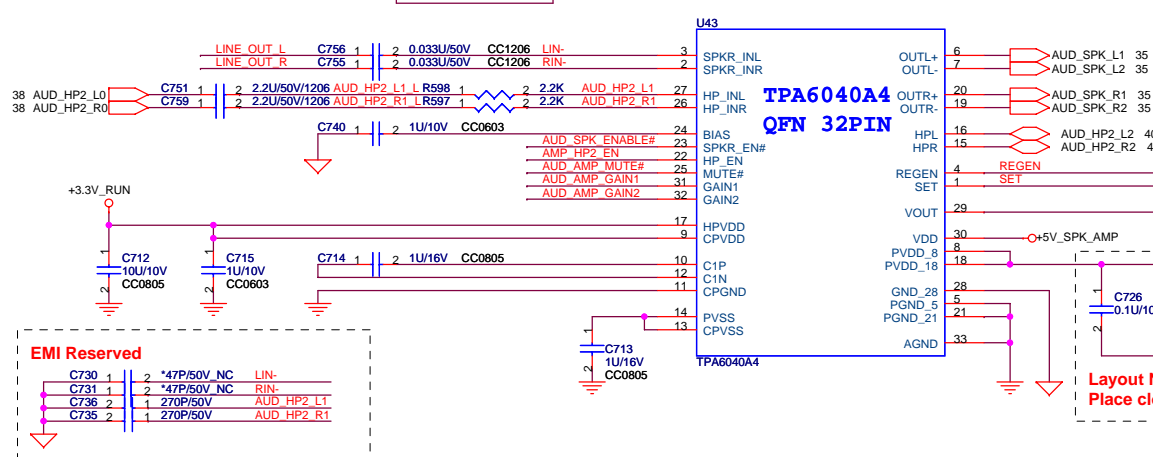
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



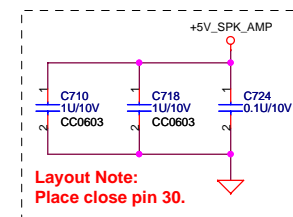
Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.



7/01: Populate according to EMI request!



For MAX9789A, depop Cap., pop 0 ohm.



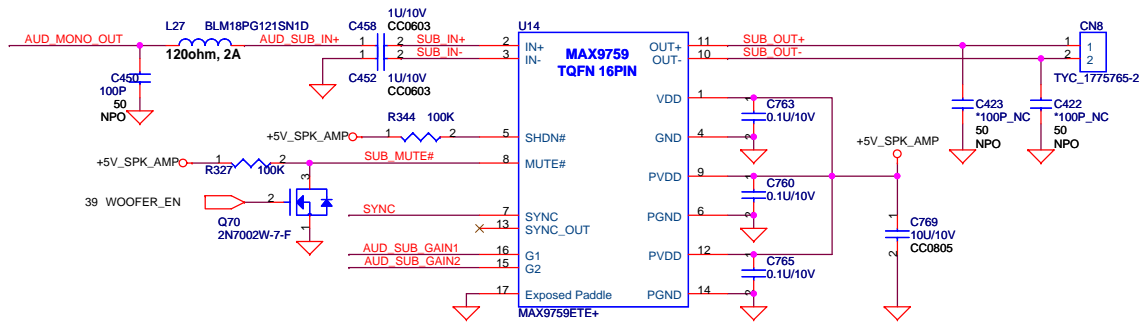
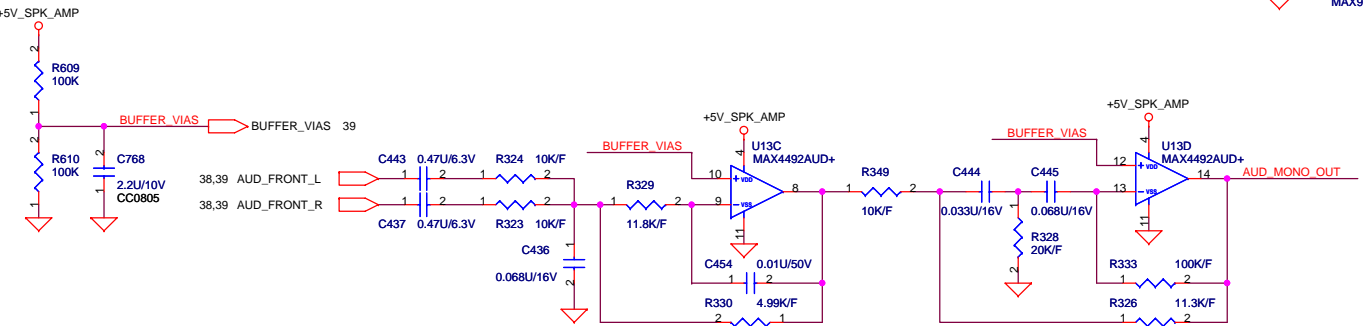
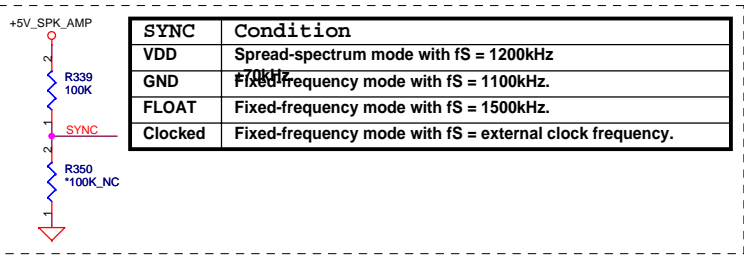
Layout Note:
Place close pin 30.

Layout Note:
Place close to pin 18.

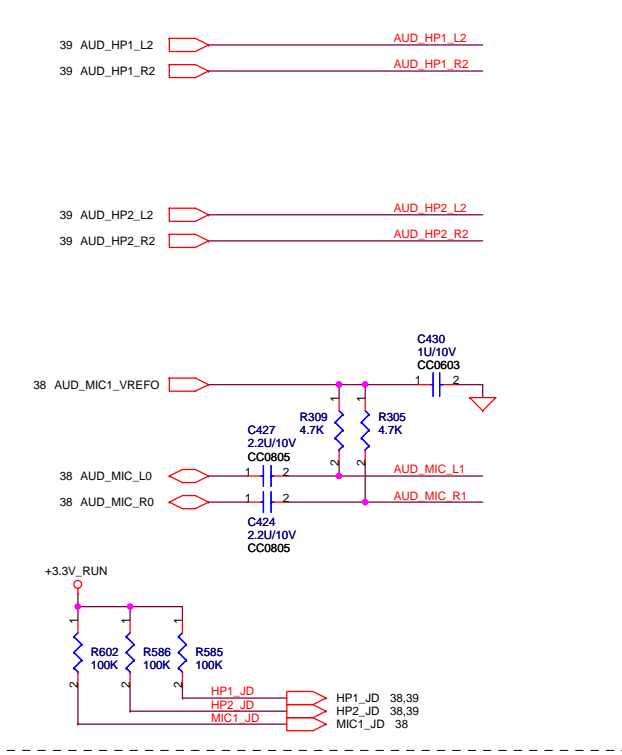
Layout Note:
Place close TPA6040.



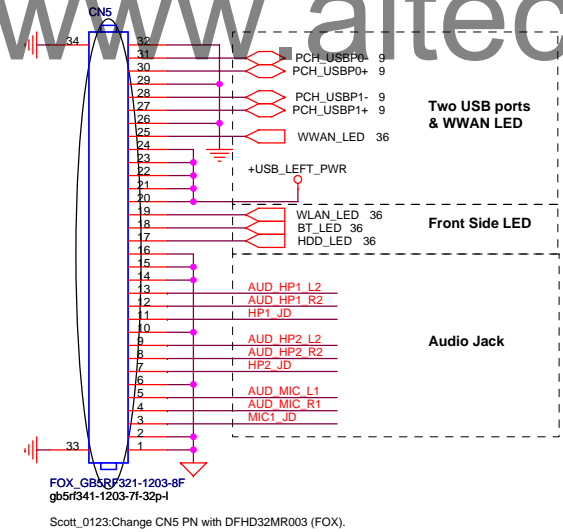
INTERNAL SUBWOOFER AMP



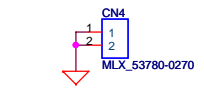
Ambient Parts of Headphone & MIC Jack



To IB(IO Board) connector



Adding additional AGND

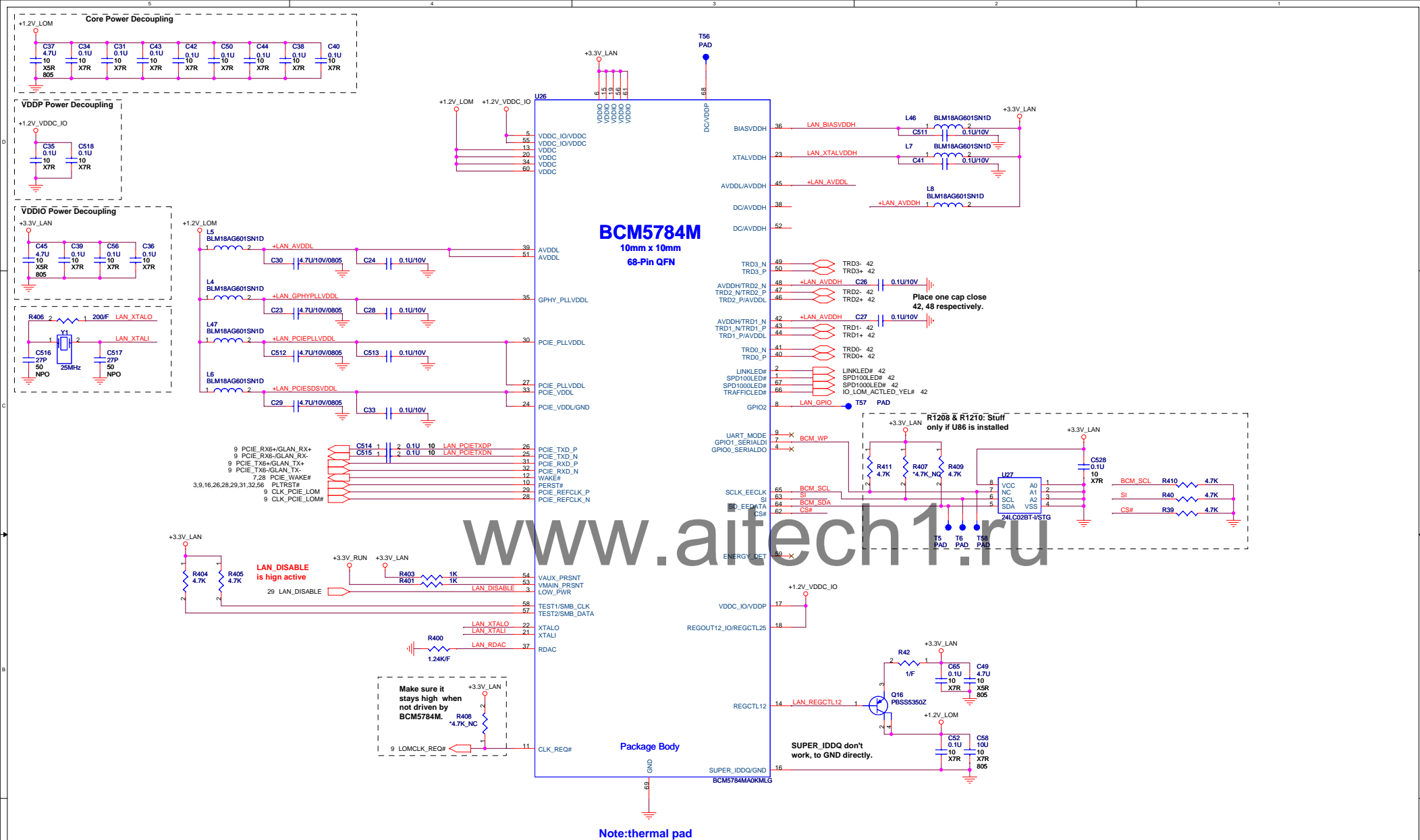


QUANTA COMPUTER logo and title block.

Title: IB CONN & SUBWOOFER

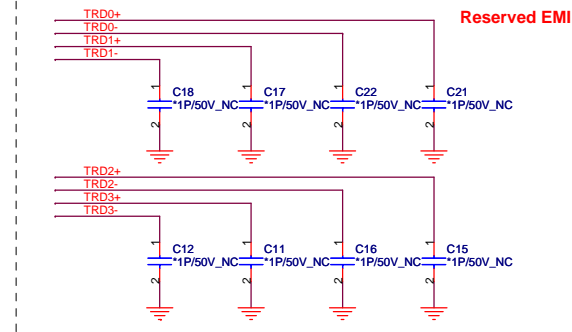
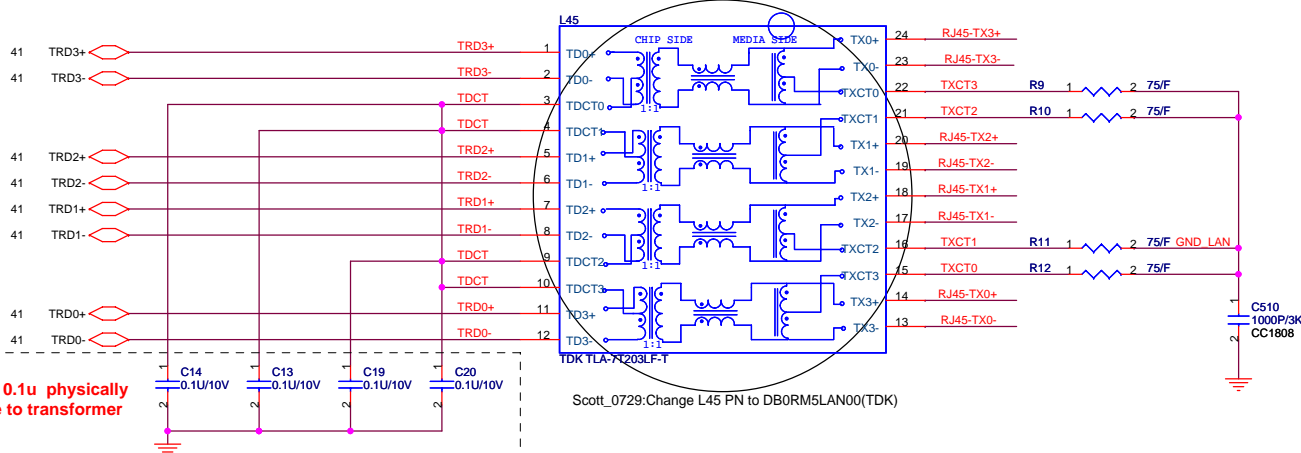
Size: Document Number RM5B Rev 3B

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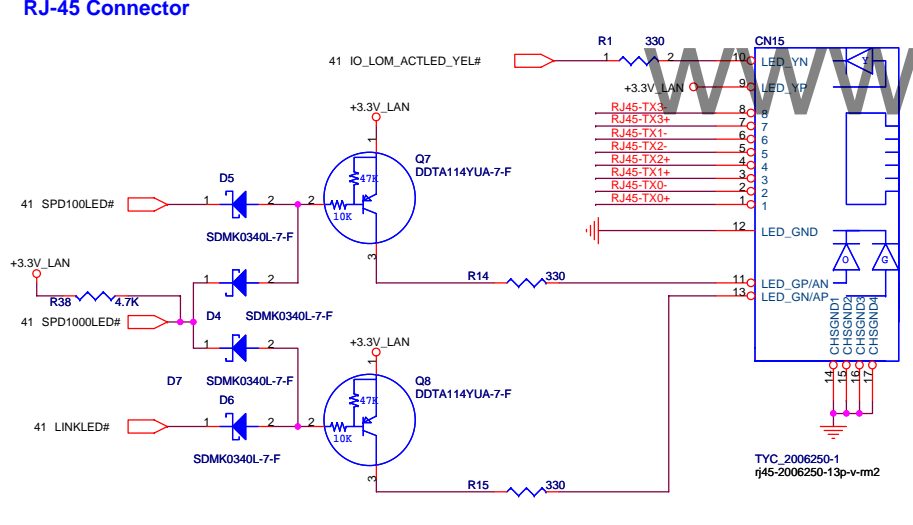


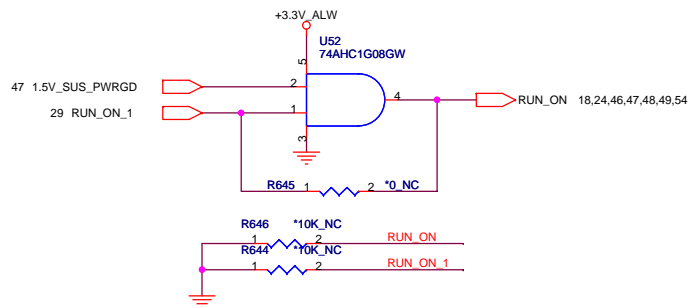
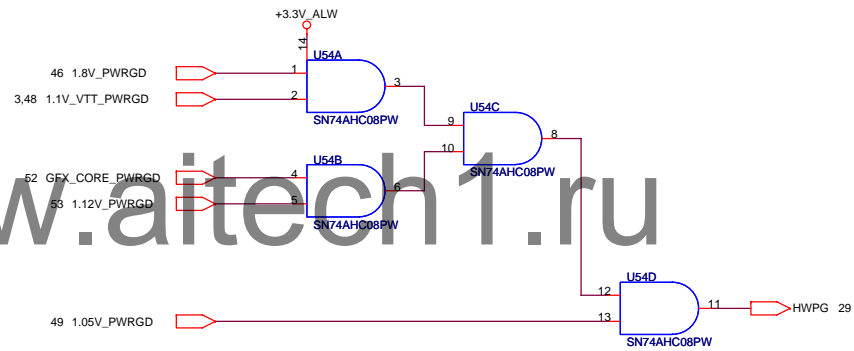
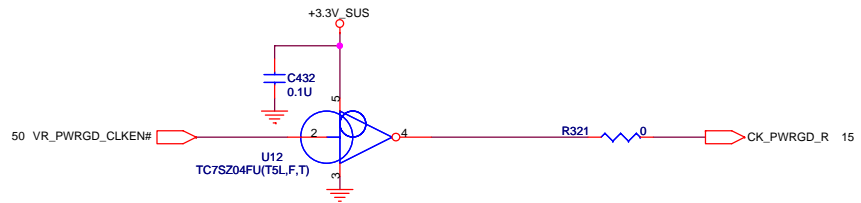
TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



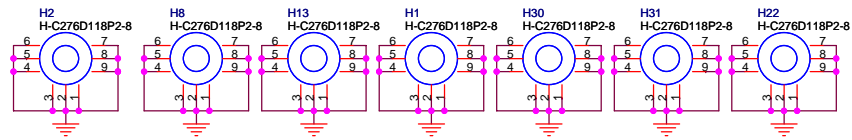
RJ-45 Connector



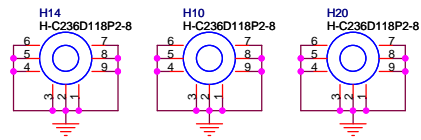


Title		
System Reset Circuit		
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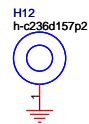
H-C276D118P2-8 * 7



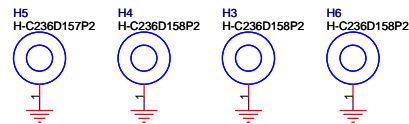
H-C236D118P2-8 * 3



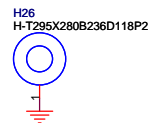
h-c236d197p2 * 1



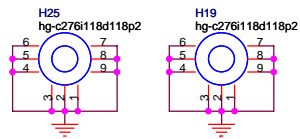
H-C236D158P2 * 4



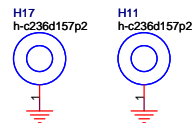
H-T295X280B236D118P2 * 1



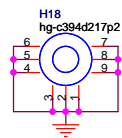
hg-c276i118d118p2 * 2



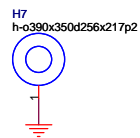
h-c236d157p2 * 2



h-c394d260p2 * 1



H-C394D260P2-8 * 1



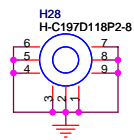
Scott_0731: change H7 & H18 footprint as ME change

Scott_0812:Delete H7 Pin2~Pin9 for layout requite.

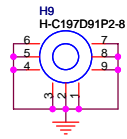
h-c236d236n * 2



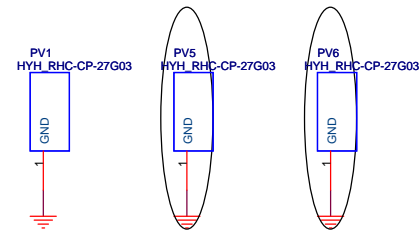
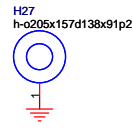
H-C197D118P2-8 * 1



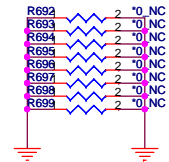
H-C197D91P2-8 * 1



h-o205x157d138x91p2 * 1



Scott_0701:: Added PV6 according to EMI's suggestion

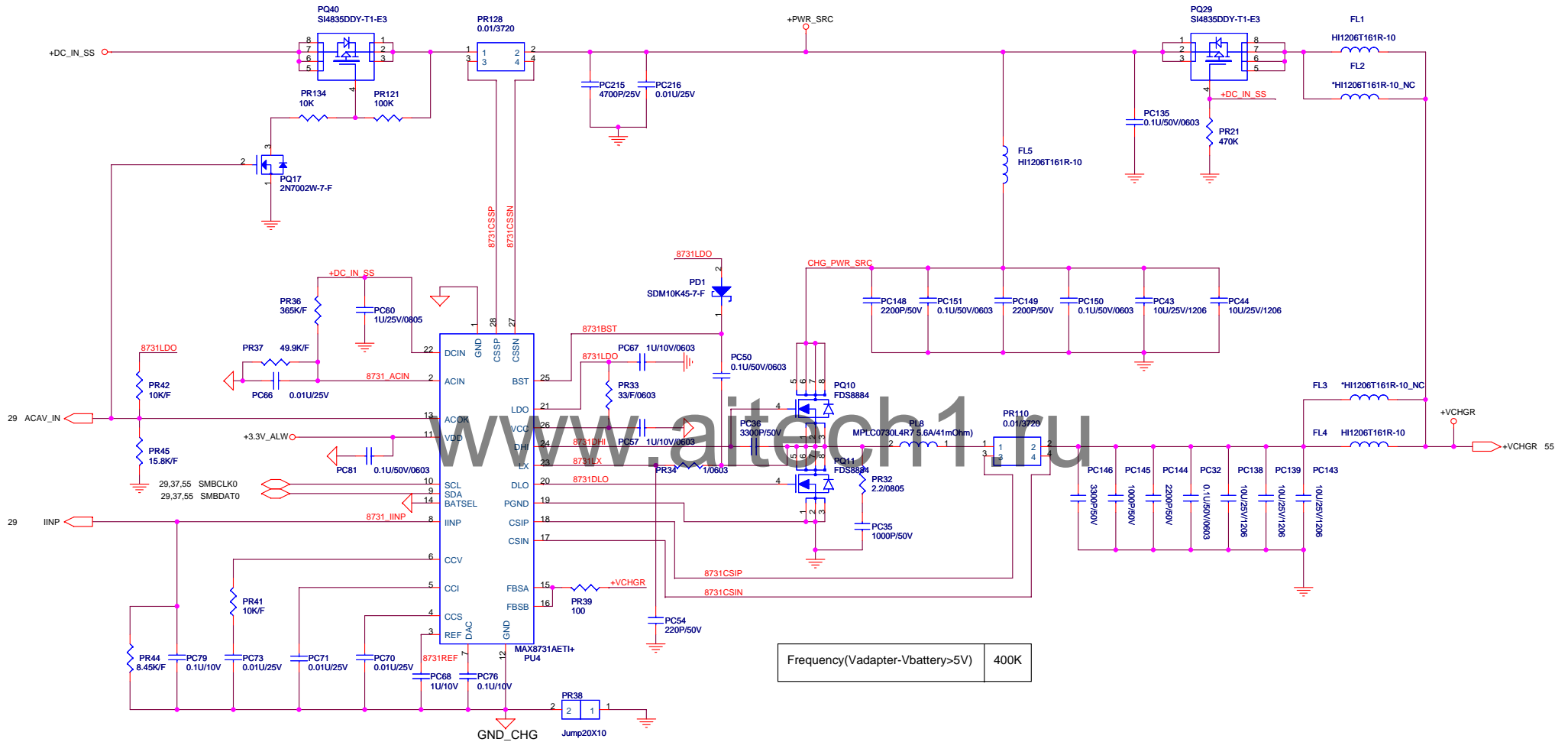


Scott_0703:Add 8pcs 0ohm resistors R692~R699 for thermal issue as EMI concern.

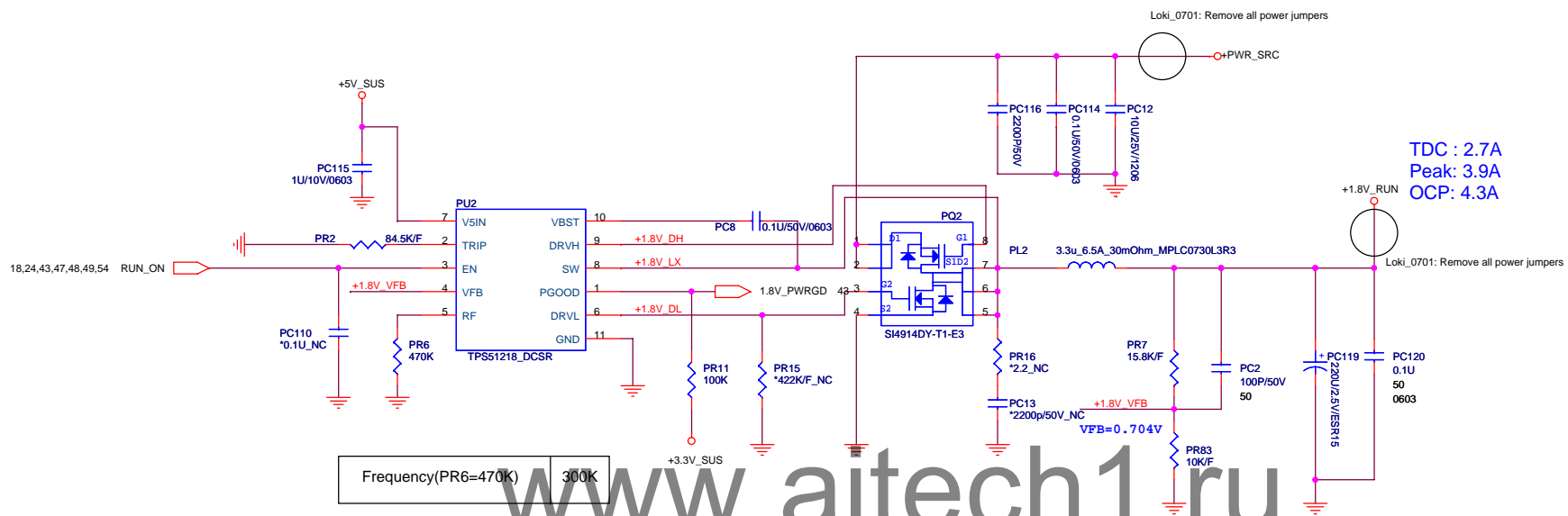
Scott_0707: Reserver R692~R699.



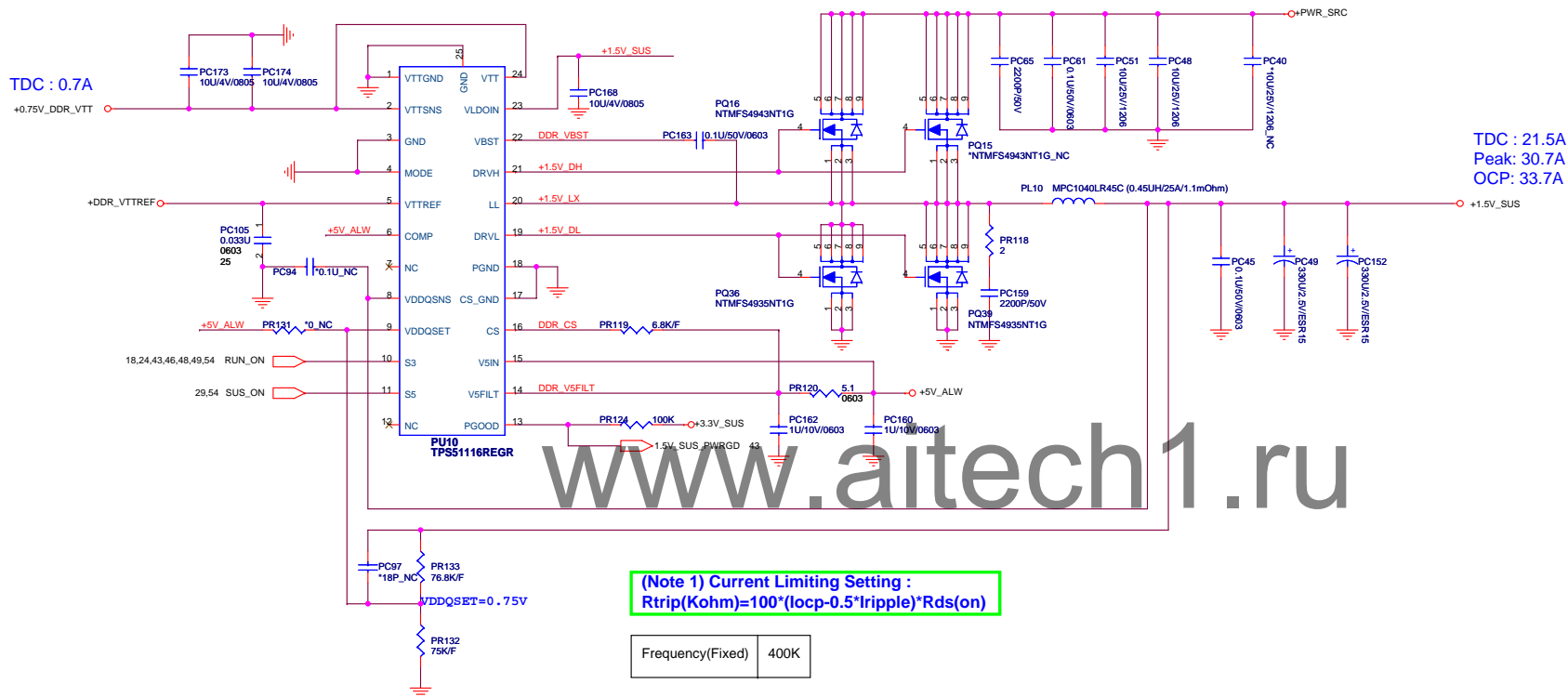
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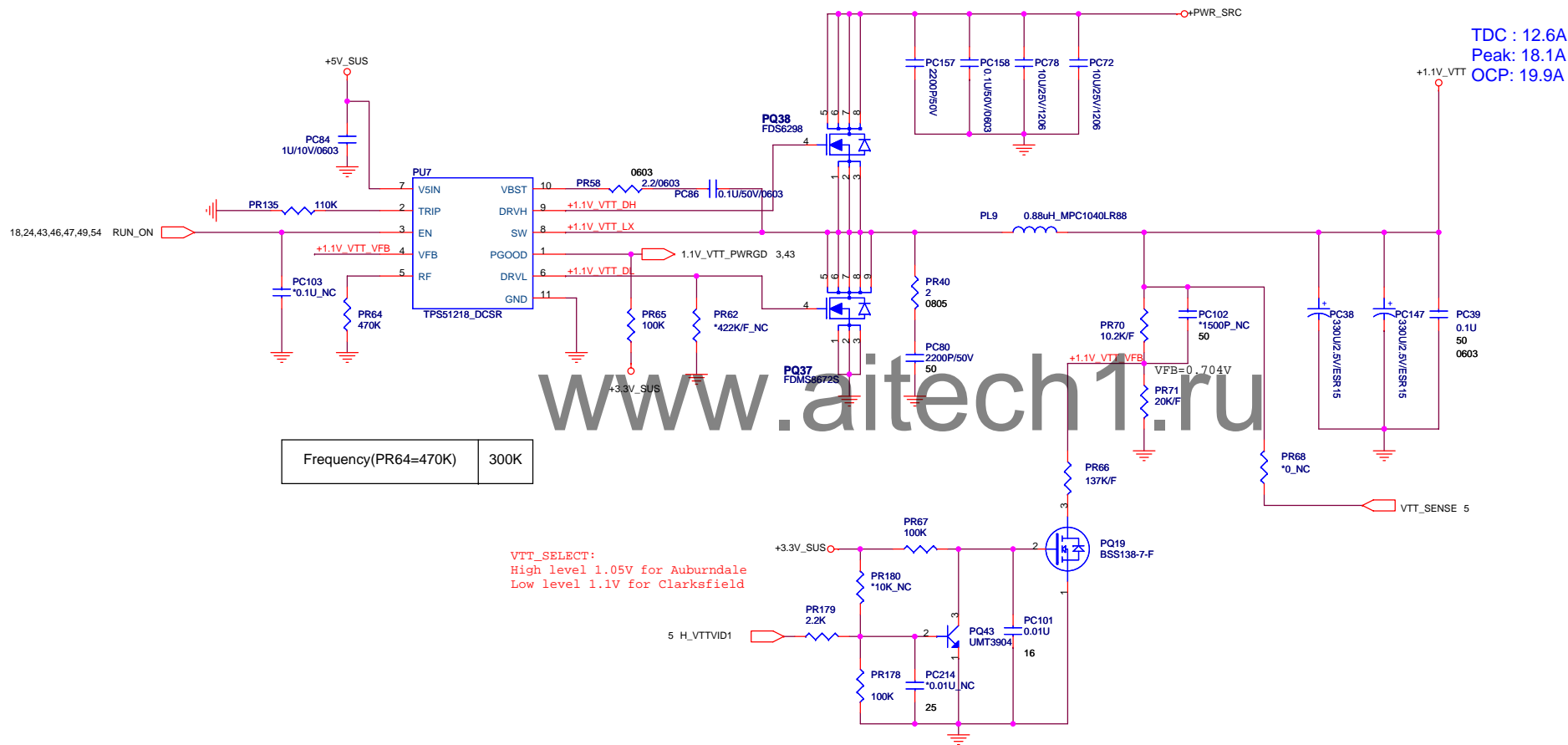


Title				CHARGER (MAX8731A)			
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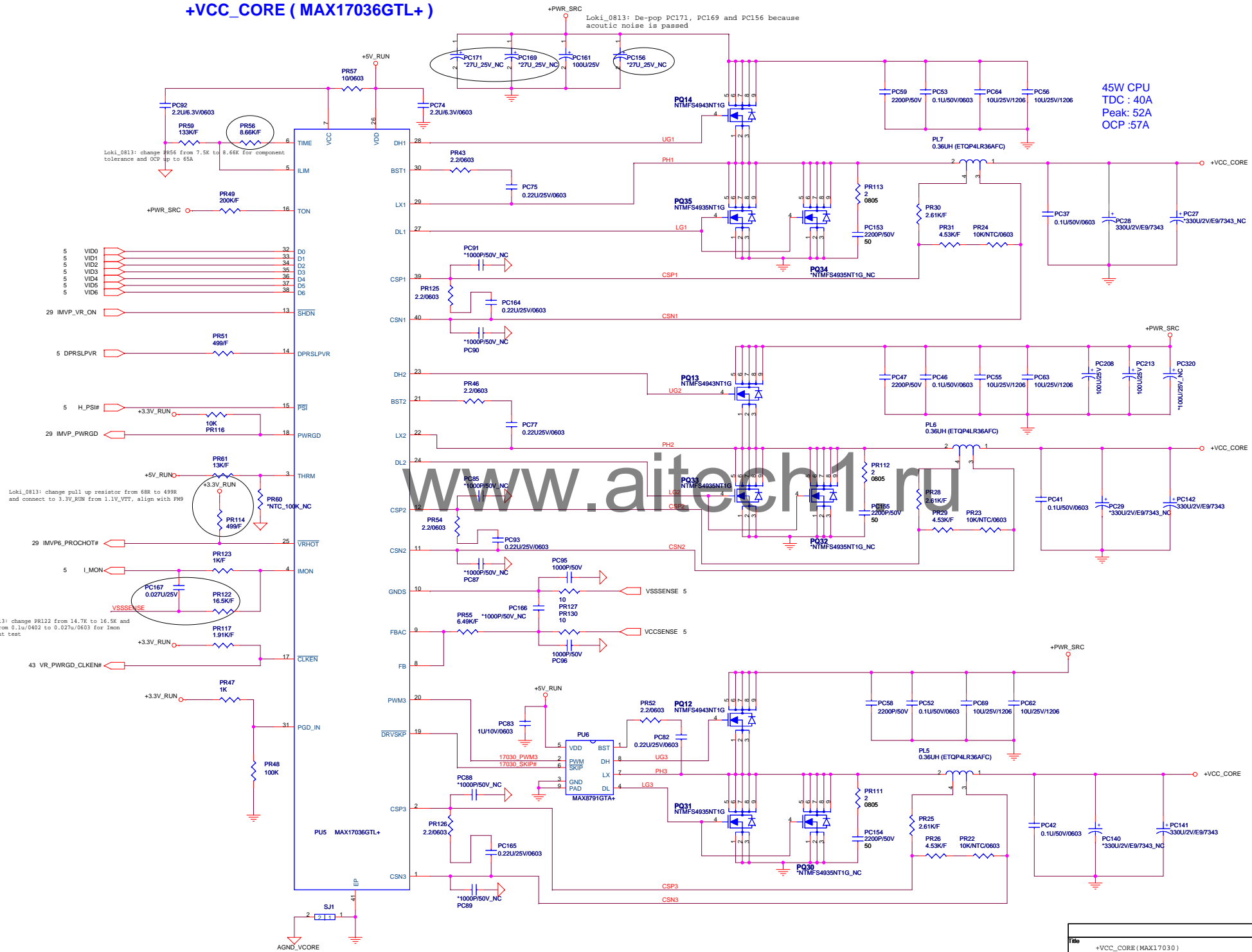


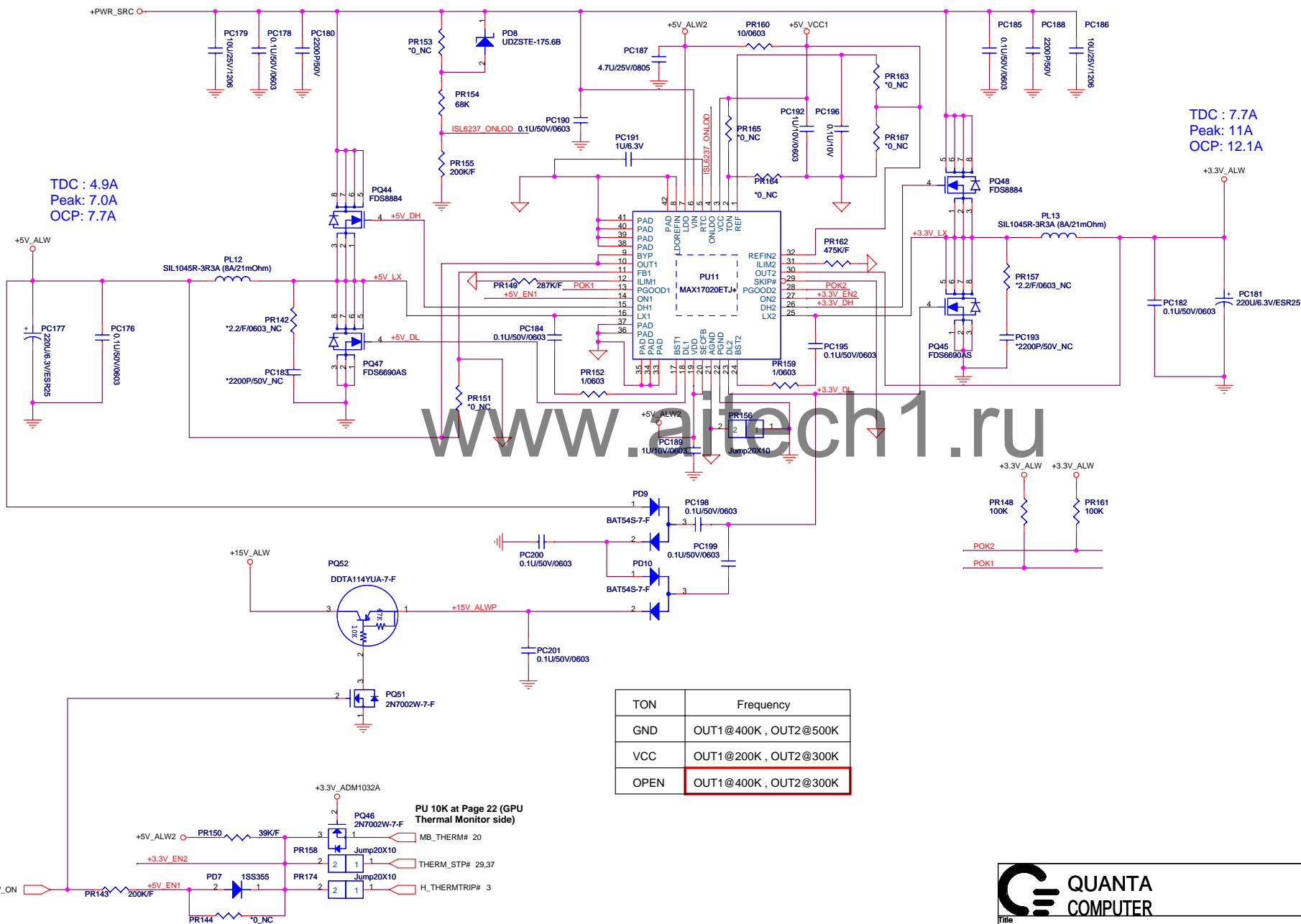
Title		
+1.8V_RUN(TPS51218)		
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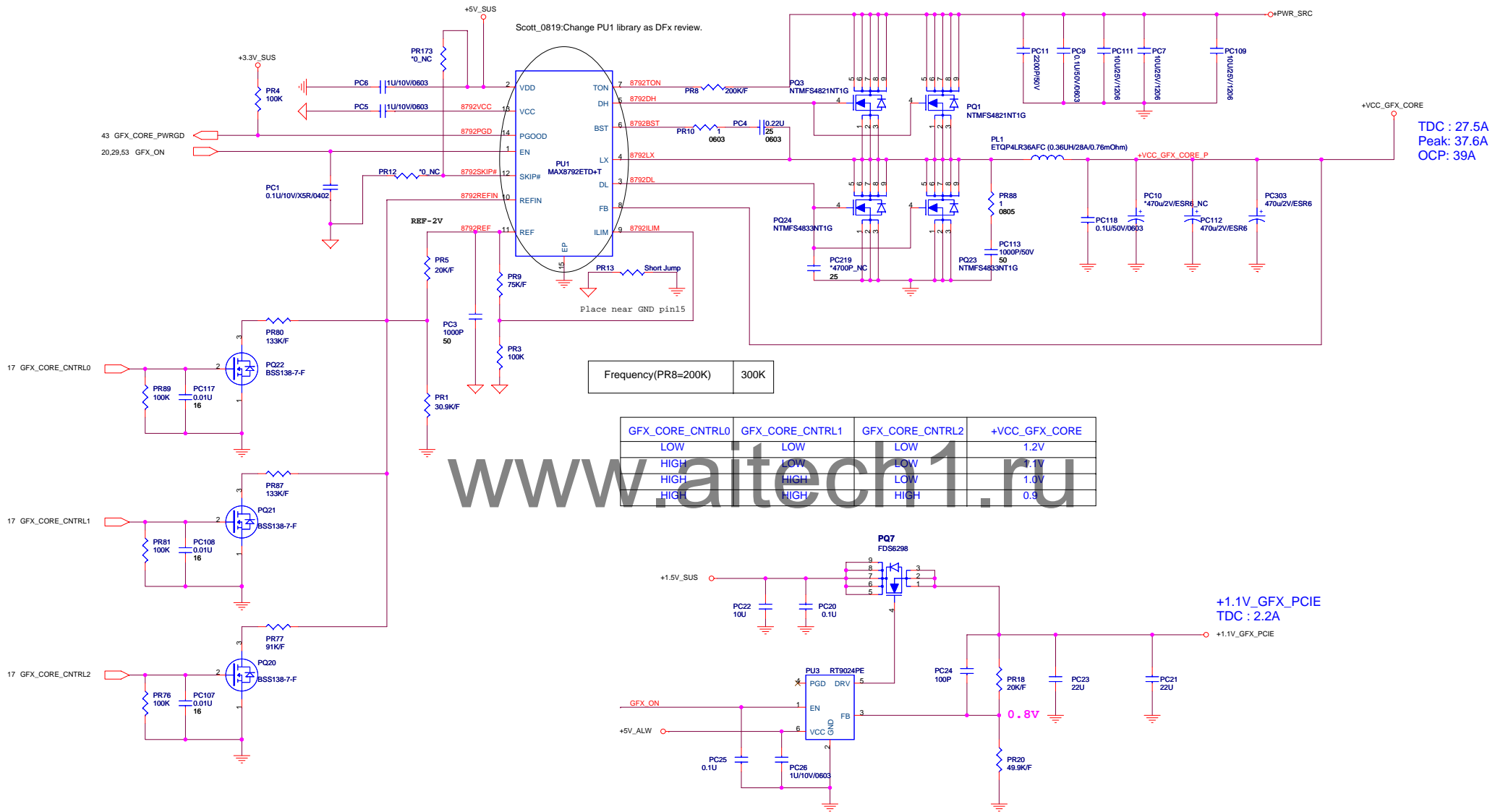


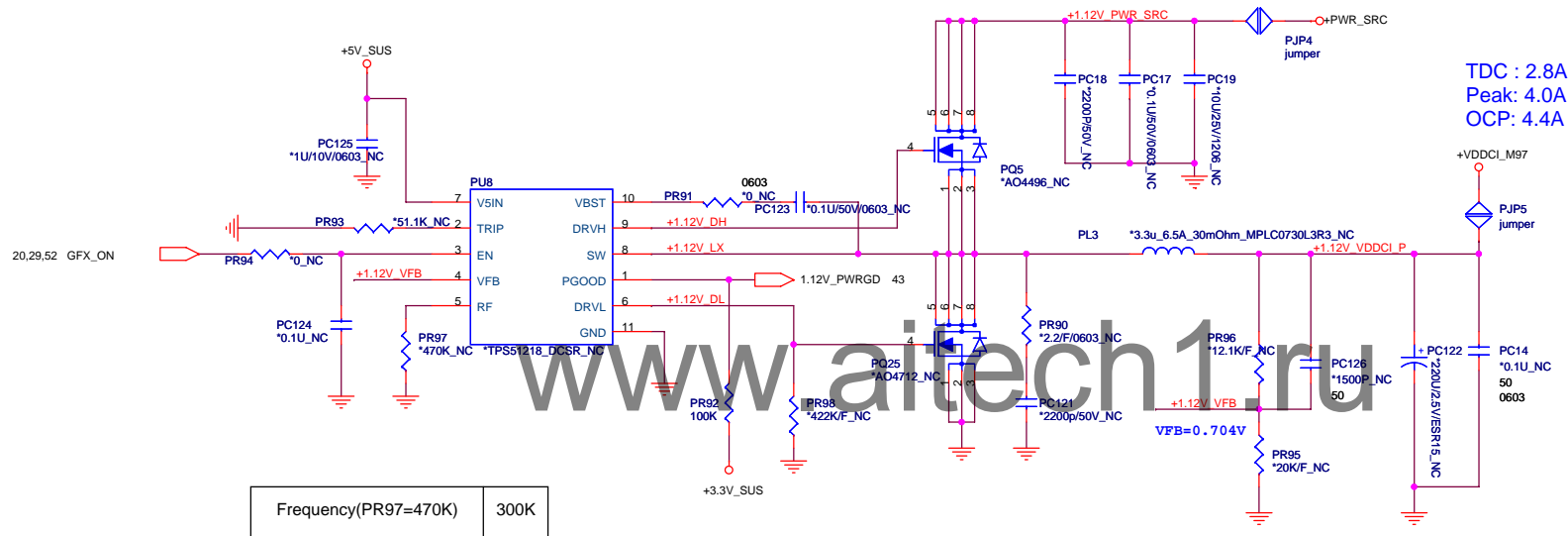


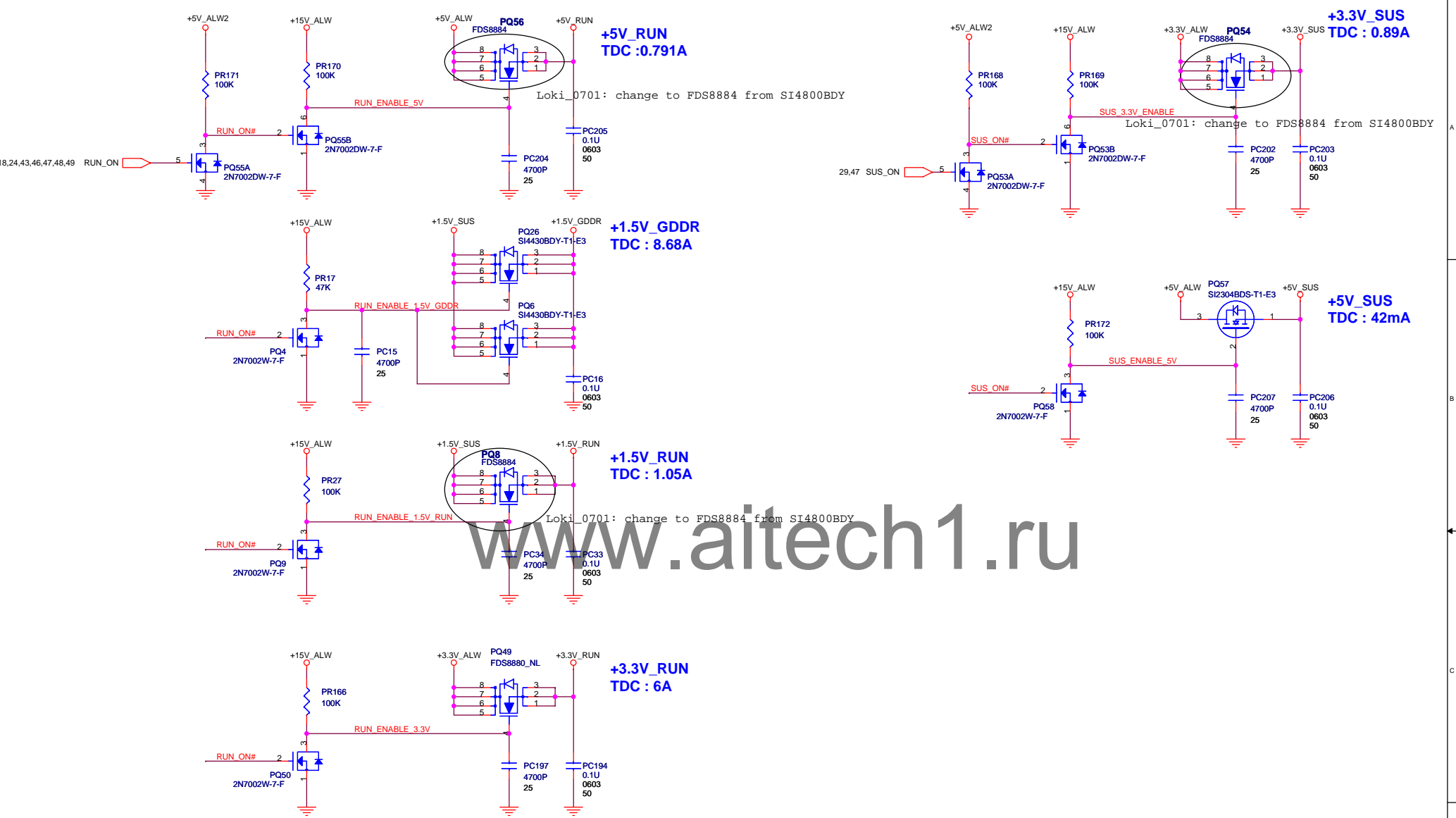
+VCC_CORE (MAX17036GTL+)



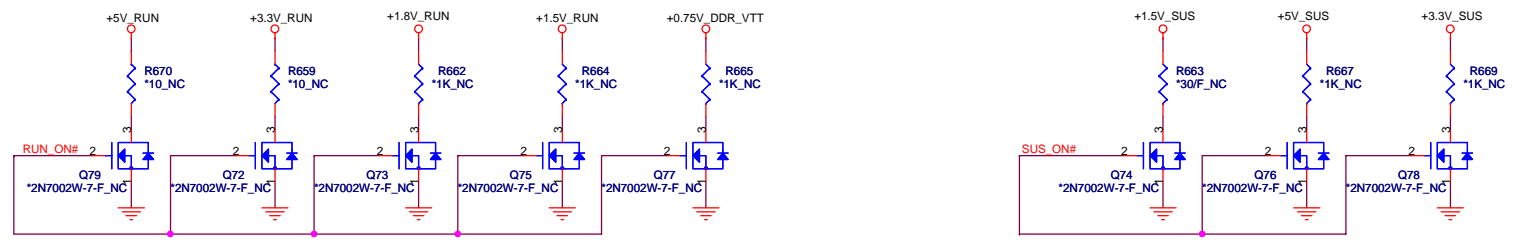






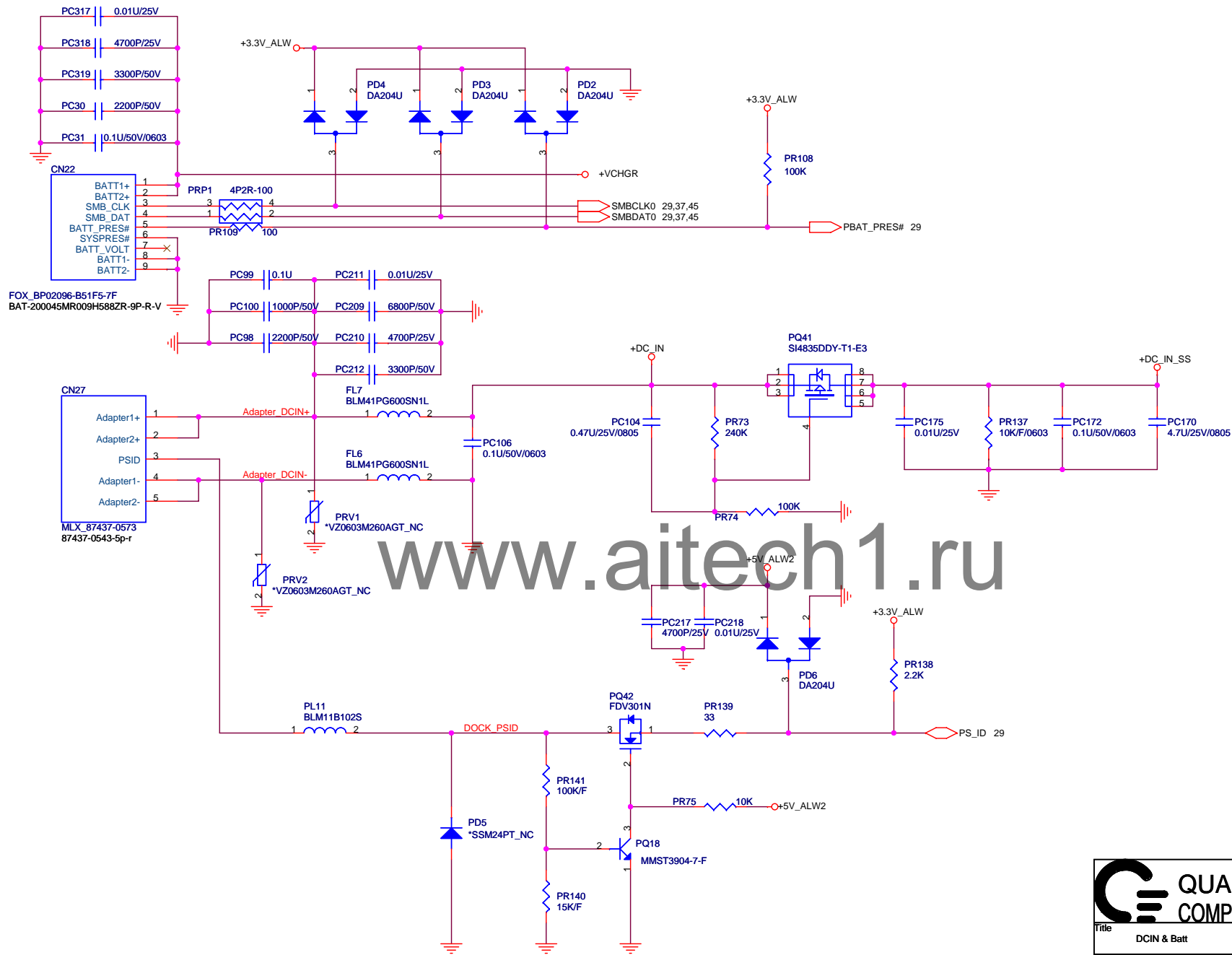


Reserve discharge path



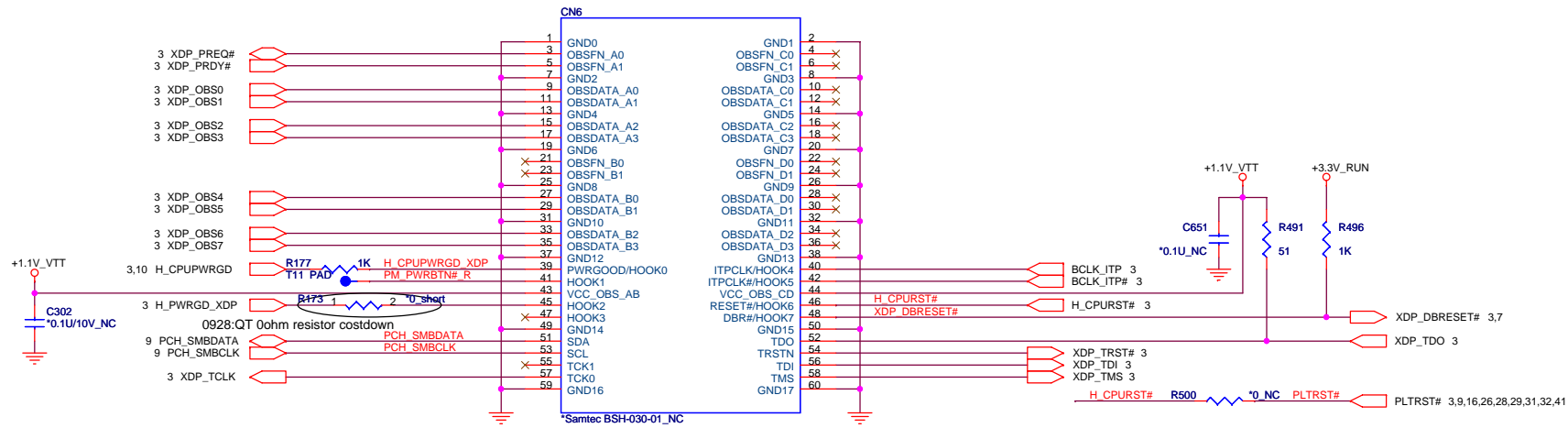
QUANTA
COMPUTER

Title RUN POWER SW		
Size RMSB	Document Number	Rev 3B
Date: Thursday, October 01, 2009	Sheet 54	of 61



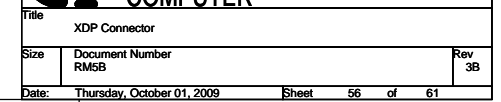
Title		
DCIN & Batt		
Size	Document Number	Rev
	RM5B	3B
Date:	Thursday, October 01, 2009	Sheet 55 of 61

CN6	
GND0	GND1
OBSFN_A0	OBSFN_C0
OBSFN_A1	OBSFN_C1
GND2	GND3
OBSDATA_A0	OBSDATA_C0
OBSDATA_A1	OBSDATA_C1
GND4	GND5
OBSDATA_A2	OBSDATA_C2
OBSDATA_A3	OBSDATA_C3
GND6	GND7
OBSFN_B0	OBSFN_D0
OBSFN_B1	OBSFN_D1
GND8	GND9
OBSDATA_B0	OBSDATA_D0
OBSDATA_B1	OBSDATA_D1
GND10	GND11
OBSDATA_B2	OBSDATA_D2
OBSDATA_B3	OBSDATA_D3
GND12	GND13
PWRGOOD/HOOK0	ITPCLK/HOOK4
H00K1	ITPCLK/H00K5
VCC_OBS_AB	VCC_OBS_C0
H00K2	RESET/H00K6
H00K3	DBR/H00K7
GND14	GND15
SDA	TDO
SCIL	TRSTIN
TCK1	TDI
TCK0	TMS
GND16	GND17

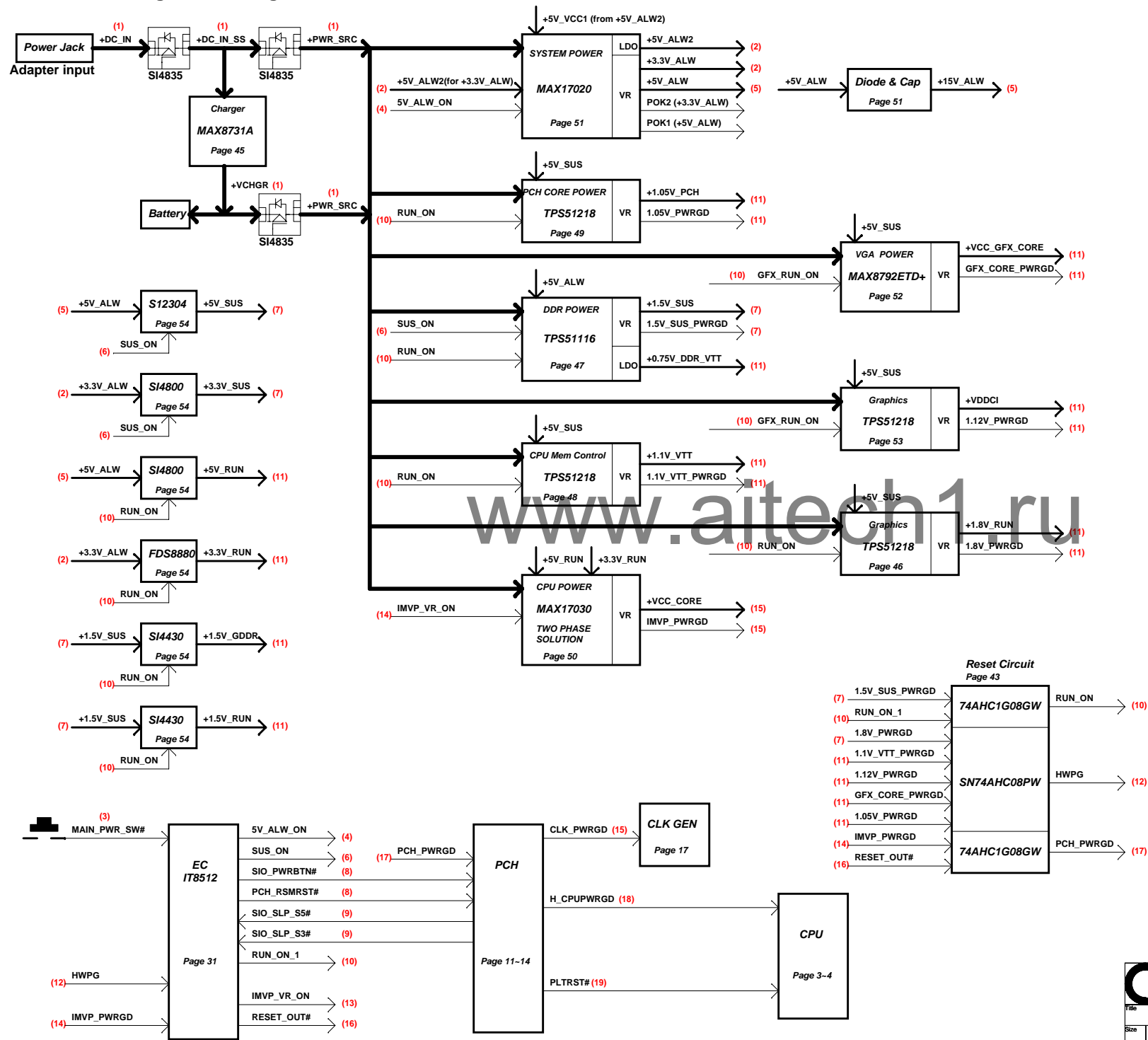


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DEL PCH XDP as FM9 confirmed with Intel that its not necessary!

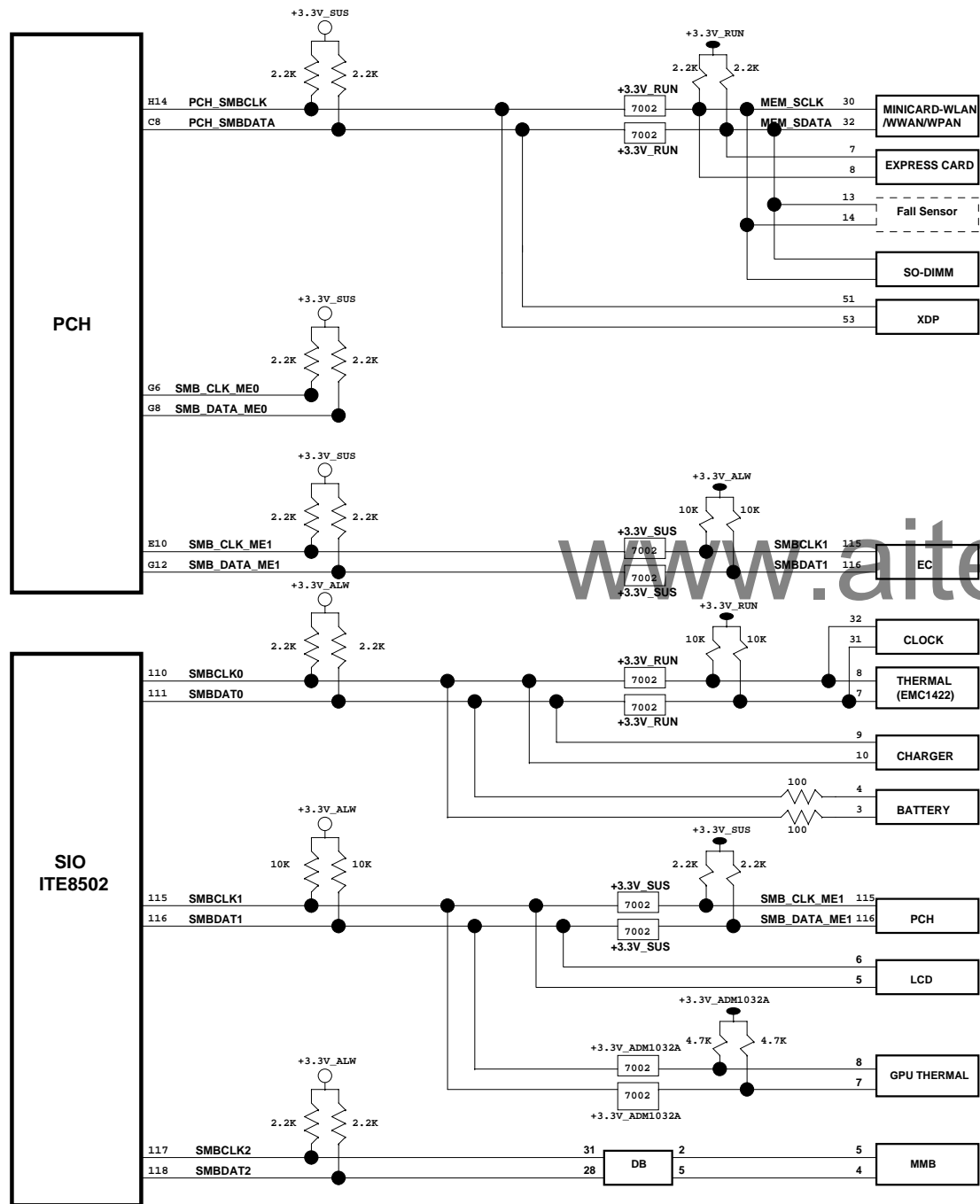


RM5 Power Design Block Diagram 2009/02/25



- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
- Bat : +VCHGR -> +PWR_SRC
- (2) +5V_ALW2, +3.3V_ALW
- (3) MAIN_PWR_SW#
- (4) 5V_ALW_ON
- (5) +5V_ALW -> +15V_ALW
- (6) SUS_ON
- (7) All SUS power & PWRGD
- (8) SIO_PWRBTN#, PCH_RSMRST#
- (9) SIO_SLP_S5#, SIO_SLP_S3#
- (10) RUN_ON_1, RUN_ON, GFX_RUN_ON
- (11) All RUN power & PWRGD
- (12) HWP
- (13) IMVP_VR_ON
- (14) IMVP_PWRGD
- (15) CLK_PWRGD
- (16) RESET_OUT#
- (17) PCH_PWRGD
- (18) H_CPUPWRGD
- (19) PLTRST#





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POWER STATES

State \ Signal	SLP_ S3#	SLP_ S4#	SLP_ S5#	S4_ STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	N/A	HIGH	N/A	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	N/A	HIGH	N/A	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	N/A	HIGH	N/A	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	N/A	LOW	N/A	ON	OFF	OFF	OFF

PM TABLE

power plane \ State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +CPU_PWR_SRC +5V_ALW2 +MMB_PWR +3.3V_ALW	+5V_ALW +15V_ALW +5V_SUS +3.3V_SUS +3.3V_LAN +3.3V_CARDAUX +1.8V_SUS +1.5V_SUS	+VCC_CORE +0.75V_DDR_VTT +1.05V_PCH +1.1V_GFX_PCIE +1.2V_LOM +1.5V_RUN +1.5V_CARD +1.8V_RUN +3.3V_RUN +3.3V_DELAY +3.3V_R5C833	+3.3V_RUN_CARD +3.3V_CARD +5V_RUN +LCDVCC +5V_HDD +5V_MOD +5V_SPK_AMP +VDDA +GFX_PWR_SRC
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	OFF	OFF
S5 & S4 with AC or BAT	ON	ON	OFF	OFF	OFF
no AC/Battery	ON	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
NONE			

PCH IBEX PEAK-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair Bottom / left
	2	USB W/ E-SATA port
	3	Reserved
	4	Mini Card (WLAN)
	5	Mini Card (WWAN)
	6	Reserved
	7	Reserved
	8	Mini Card (WPAN)
	9	TV
	10	Express Card
	11	Camera
PCH IBEX PEAK-M	PCI EXPRESS	DESTINATION
	Lane 1	Mini Card-1 WWAN
	Lane 2	Mini Card-2 WLAN
	Lane 3	Mini Card-3 WPAN
	Lane 4	Express Card
	Lane 5	Cardreader
	Lane 6	LOM